Micro-grid Inverter Module

PEK-530

User Manual

GW INSTEK PART NO. 82EK-11000M01

ISO-9001 認證企業

GW INSTEK

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Table of Contents

Introduction

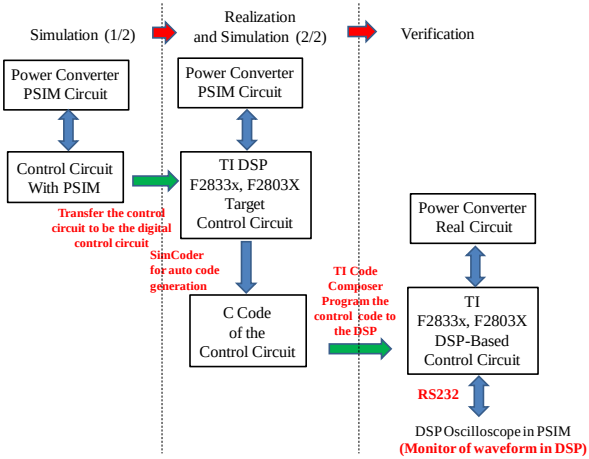
As the figure 0.1 shown, PEK-530, the Micro-grid Inverter Module, which is based on the structure of 2 sets of Three Phase Full Bridge Inverter with fully digital control system. The purpose of it, as shown in the figure 0.2, is to provide a learning platform for power converter of specifically digital control, having users, via PSIM software, to understand the principle, analysis as well as design of power converter through simulating process. More than that, it helps convert, via SimCoder tool of PSIM, control circuit into digital control and proceed to simulation with the circuit of DSP, eventually burning the control program, through simulating verification, in the DSP chip. Also, it precisely verifies the accuracy of designed circuit and controller via control and communication of DSP.

Figure 0.1

Micro-grid inverter experiment module

Figure 0.2

The process in details



Thre are 6 experiments can be fulfilled by PEK-530 as follows:

1. Three Phase SVPWM Inverter
2. Three Phase Stand-alone Inverter
3. Three Phase Grid-connected Inverter
4. PQ Control of Three-phase Grid-connected inverter
5. P-ω and Q-V Droop control of Three Phase Stand-alone Inverter
6. Parallel Operation of Multiple Stand-alone Inverters with Virtual Impedance and Drop Control Method

In addition to PEK-530, it is required to utilize PEK-005A auxiliary power module as figure 0.3 shown and PEK-006 JTAG burning module as figure 0.4 shown for experiments. Also, PTS-5000 experiment platform as figure 0.5 shown is necessary for completing the experiments.

Figure 0.3

Auxiliary power module

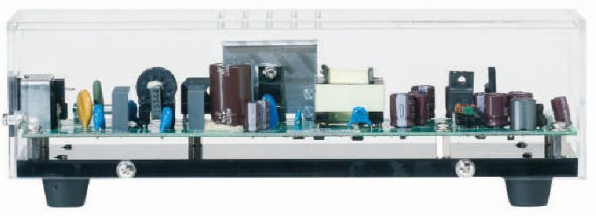


Figure 0.4

JTAG burning module

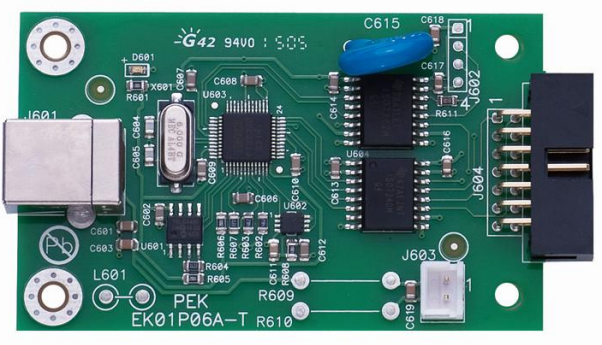


Figure 0.5

PTS-5000 experiment platform

The DSP I/O pin configuration of PEK-530 is shown as the figure 0.6. Refer to the appendix A for the circuit diagrams of PEK-530, which can be divided into power circuit, sensing circuit, drive circuit and protection circuit. The sensing circuit is further divided into 2 sections; one is for test point measurement, and the other one is for feedback DSP control, both of which have varied attenuation amplifications individually as the following table 0-1 and table 0-2 shown.

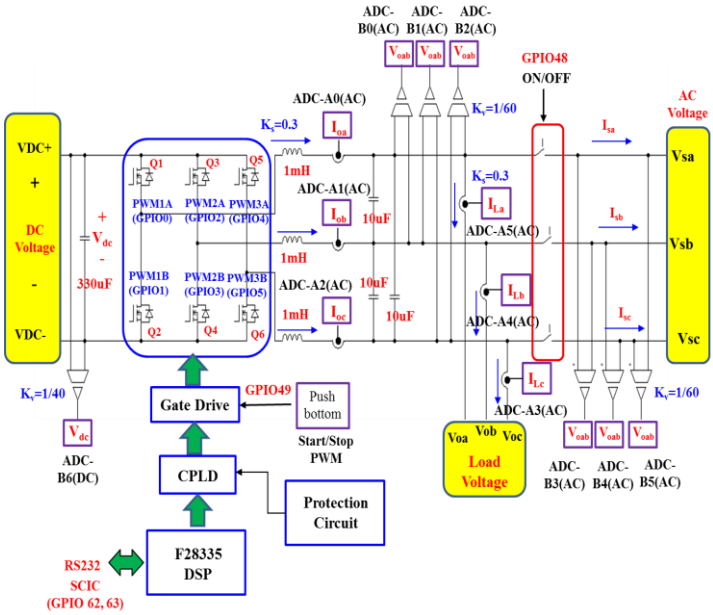


Figure 0.6 I/O configuration

Table 0.1 PEK-530 test point measurement ratio

	Sensing item	Sensing ratio
1	DC link voltage (VDC)	0.0196
2	Inverter A phase output current (IO-A)	0.4768
3	Inverter B phase output current (IO-B)	0.4768
4	Inverter C phase output current (IO-C)	0.4768
5	Inverter A phase load current (IL-A)	0.4768
6	Inverter B phase load current (IL-B)	0.4768
7	Inverter C phase load current (IL-C)	0.4768
8	Inverter output AB arm line voltage (VO-AB)	0.0287
9	Inverter output BC arm line voltage (VO-BC)	0.0287
10	Inverter output CA arm line voltage (VO-CA)	0.0287
11	Grid-connected AB arm line voltage (VS-AB)	0.0287
12	Grid-connected BC arm line voltage (VS-BC)	0.0287
13	Grid-connected CA arm line voltage (VS-CA)	0.0287

Table 0.2 PEK-530 DSP feedback ratio

	Sensing item	Sensing ratio
1	DC link voltage (VDC)	0.0249
2	Inverter A phase output current (IO-A)	0.2996
3	Inverter B phase output current (IO-B)	0.2996
4	Inverter C phase output current (IO-C)	0.2996
5	Inverter A phase load current (IL-A)	0.2996
6	Inverter B phase load current (IL-B)	0.2996
7	Inverter C phase load current (IL-C)	0.2996
8	Inverter output AB arm line voltage (VO-AB)	0.0169
9	Inverter output BC arm line voltage (VO-BC)	0.0169
10	Inverter output CA arm line voltage (VO-CA)	0.0169
11	Grid-connected AB arm line voltage (VS-AB)	0.0169
12	Grid-connected BC arm line voltage (VS-BC)	0.0169
13	Grid-connected CA arm line voltage (VS-CA)	0.0169

The Description on Chapters

See the chaper arrangements as follows

Introduction	Briefly describes the experimental method, experimental items and circuit setup. It also explains the contents of each chapter.
Experiment 1 Three Phase SVPWM inverter	Learns the theories of three-phase SPWM and SVPWM, the measuring method of voltage and current for PEK-530 module, the pin layout of TI F28335 DSP IC, the setting for PWM and A/D module and the method of measure and control of DSP internal signal by RS232.
Experiment 2 Three Phase Stand-alone inverter	Learns the modularization method for three-phase inverter, controller design of current and voltage loops, hardware layout followed by SimCoder programming.
Experiment 3 Three Phase Grid-connected inverter	Learns the principle and structure of three phase grid-connected inverter with the method of phase-lock loop design, the controller design of current loop and voltage loop, the hardware layout aiming at grid-connected inverter followed by SimCoder programming.
Experiment 4 PQ Control of Three Phase Grid-connected inverter	The essence of PQ control is to decouple active power and reactive power for further control, respectively. PEK-530 aims at PQ control for planning followed by SimCoder programming.
Experiment 5 P-ω and Q-V Droop control of Three Phase Stand-alone Inverter	Learns P-ω and Q-V Droop control and through PEK-530 for planning followed by SimCoder programming.

Experiment 6 Parallel Operation of Multiple Stand-alone Inverters with Virtual Impedance and Drop Control Method	Understands the parallel control method of three phase inverter, and makes 2 sets of inverters connected in parallel for control. Finally via PEK-530 for planning followed by SimCoder programming.

Experiment 1 – Three Phase SVPWM Inverter

Circuit Simulation

Inverter Specification

DC Voltage V_{DC} = 100V

F_s = 18kHz，V_{tri} = 10V_{pp} (PWM)

C_d = 330uF，L = 1mH，C = 10uF

K_s = 0.3 (AC current sensing factor)

K_v = 1/60 (DC voltage sensing factor)

K_v = 1/40 (DC voltage sensing factor)

The analogue circuit diagram based on the parameters above is as the following figure 1.1 shown:
PSIM File: PEK-530_Sim1_3P_SVPWM_Inv(60Hz)_V11.1.5_V1.1

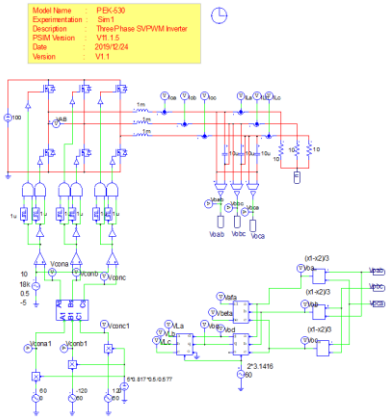


Figure 1.1 Experiment 1 PSIM analogue circuit diagram

The simulating results are shown as the figure 1.2 and 1.3:

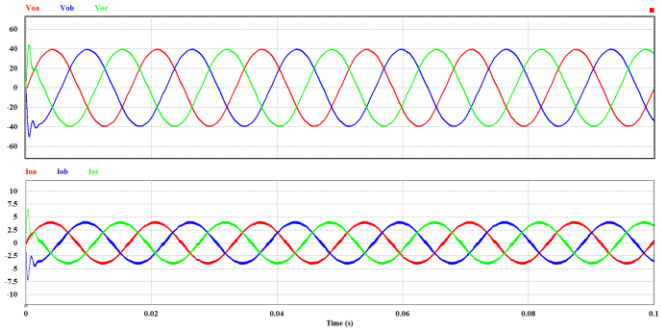


Figure 1.2 Experiment 1 analogue circuit simulation waveforms

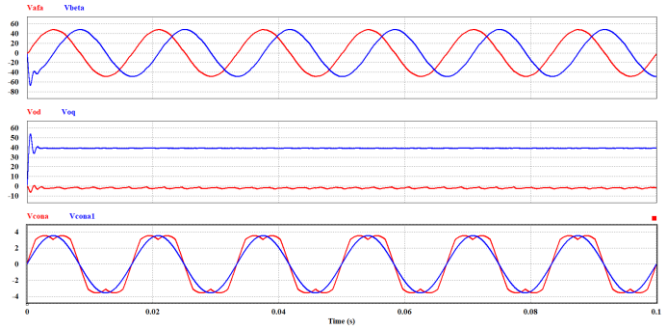


Figure 1.3 Experiment 1 analogue circuit simulation waveforms

The digital circuit diagram based on the analogue circuit is shown as the figure 1.4:
PSIM File: PEK-530_Lab1_3P_SVPWM_Inv(60Hz)_V11.1.5_V1.1

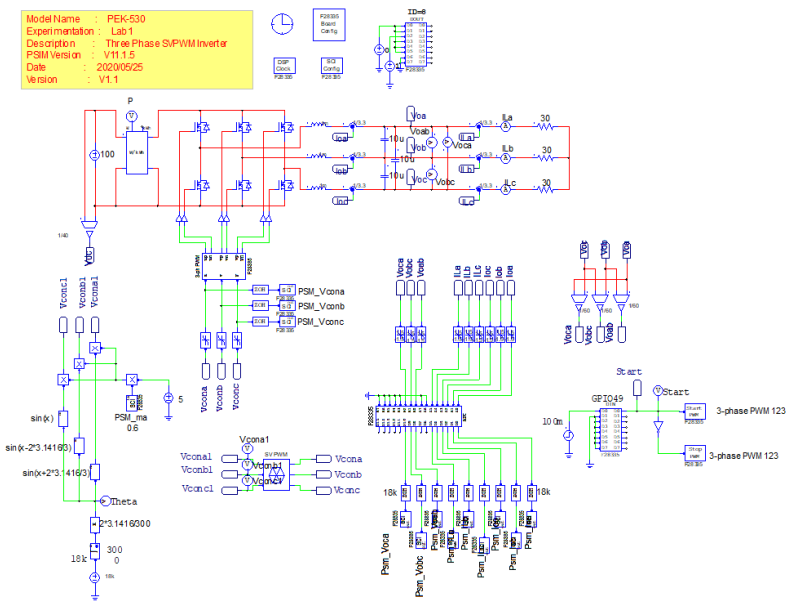


Figure 1.4 Experiment 1 PSIM digital circuit diagram

The simulating results are shown as the figure 1.5 and 1.6:

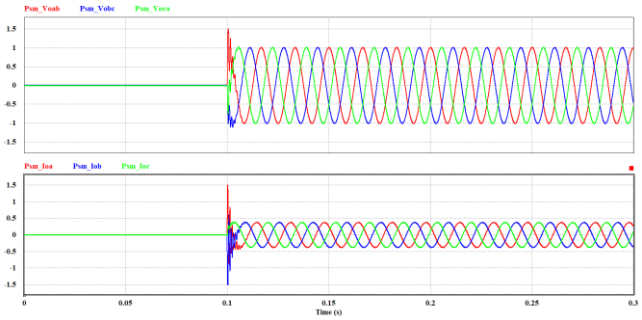


Figure 1.5 Experiment 1 digital circuit simulation waveforms

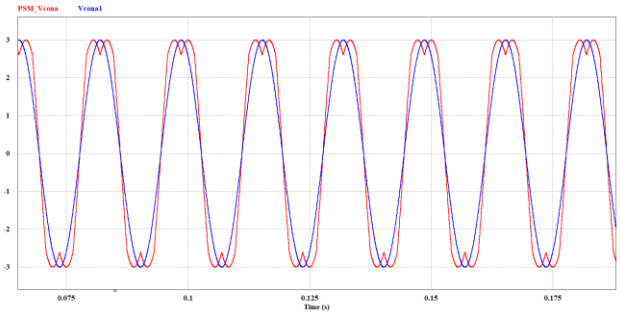


Figure 1.6 Experiment 1 digital circuit simulation waveforms

After confirming simulation, the corresponding C Code will be generated automatically via “Generate Code” of “Simulate”.

Experiment Devices

The required devices for experiment are as follows. Refer to user manuals of each device before operation:

- PEK-530 * 1
- PEK-005A * 1
- PEK-006 * 1
- PTS-5000 * 1 (with GDS-2204E, PSW160-7.2 and GPL-500)
- PC * 1

Experiment Procedure

1. The experiment wiring is shown as the figure 1.7. Please follow it to complete wiring.

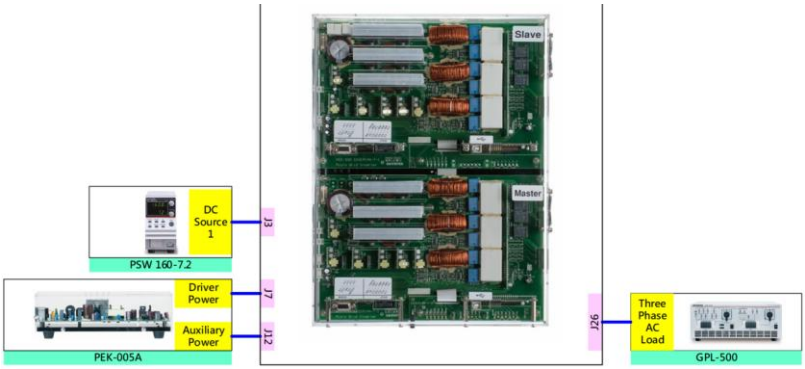


Figure 1.7 Experiment 1 wiring figure

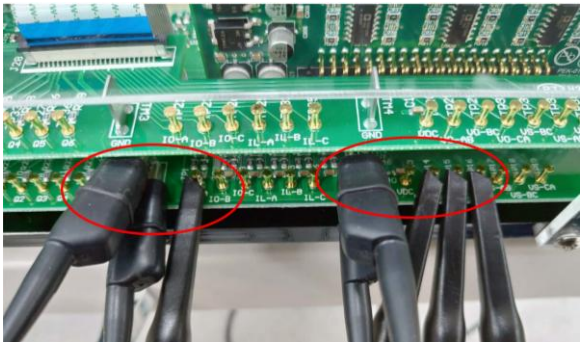
2. After wiring, make sure the PEK-530 switch is OFF followed by turning the PEK-005A switch ON. The DSP red indicator lights on as the figure 1.8 shown, which means the DSP power is steadily normal.

Figure 1.8 DSP normal status with light on

3. Refer to the appendix B for burning procedure followed by the appendix C for RS232 connection

4. Connect the test leads of oscilloscope to Vo-AB, Vo-BC and Vo-CA, respectively, followed by connecting GND of probe to the GND terminal as the figure 1.9 shown.

Figure 1.9 Oscilloscope test leads wiring

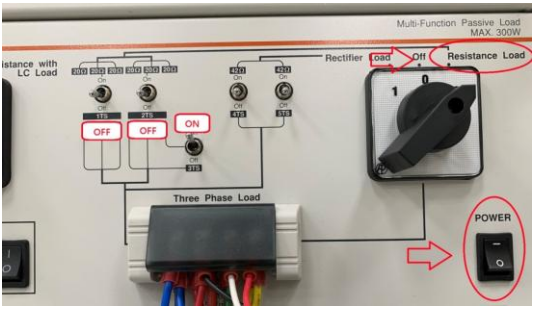


5. Refer to the figure 1.10 for the operation steps of PSW160-7.2. Power on PSW160-7.2→Click on Set key followed by adjusting voltage to 100V via voltage knob and adjusting current to 3A via current knob.

Figure 1.10 The settings of PSW

6. As the figure 1.11 shown, follow the steps below for GPL-500 operation. Power on GPL-500 → Rotate the Three Phase Lord knob to 2 (Resistance Load) → Set 1TS and 2TS as OFF, and 3TS as ON, which indicates no-load mode.

Figure 1.11 The no-load setting of GPL-500



7. After setting up and turning on PSW power output, finally turn on the switch of PEK-530

The purpose of experiment

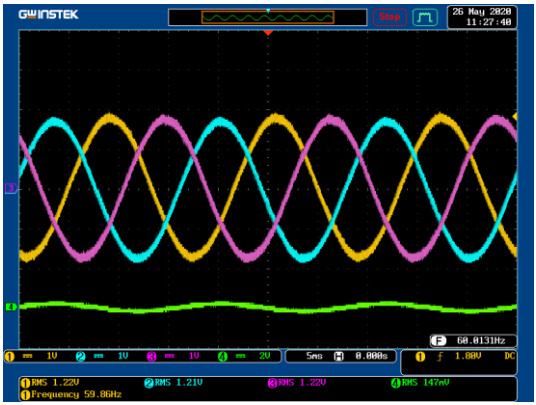
This experiment is the open loop system. We observe fluctuations of ouput voltage and current while operating under varied loads and working cycles.

The experiment result

(1) No Load

The figure 1.12 shows that when it is no-load mode, the RMS values of Vo-AB, Vo-BC and Vo-CA are 1.22V (42.509V in actual value), 1.21V (42.16V in actual value) and 1.22V (42.509V in actual value), respectively, and the RMS value of Io-A is 0.147A (0.308A in actual value).

Figure 1.12 No-load measured waveform



(2) Half Load (20Ω)

The figure 1.13 shows that 1Ts and 3TS of GPL-500 are set ON, whereas 2TS is set OFF, which indicates half load.

The figure 1.14 shows that when it is hald-load mode, the RMS value of Vo-AB, Vo-BC and Vo-CA is 1.13V (39.373V in actual value), and the RMS value of Io-A is 0.567A (1.189A in actual value).

Figure 1.13 GPL-500 half-load setting

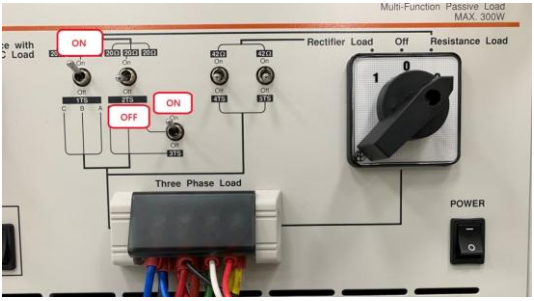
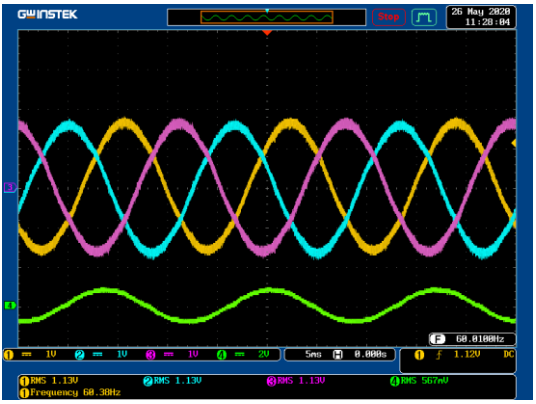


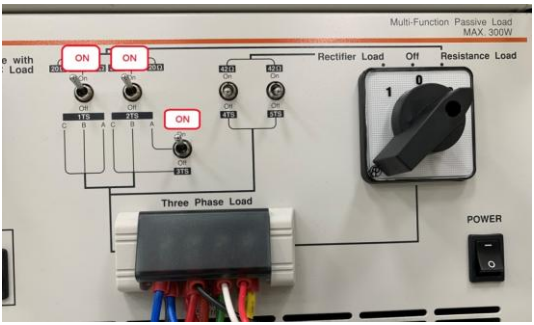
Figure 1.14 Half-load measured waveform



(3) Full Load (10Ω)

The figure 1.15 shows that 1Ts, 2Ts and 3TS of GPL-500 are set ON, which indicates full load.

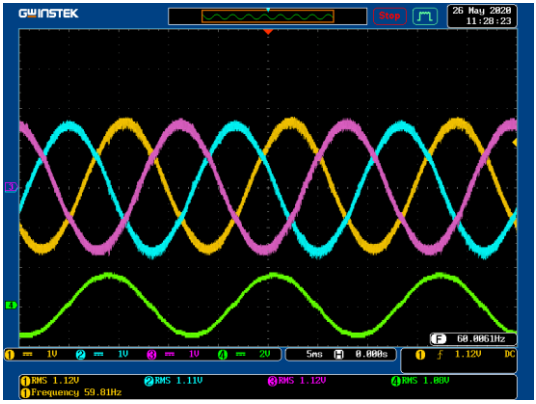
Figure 1.15 GPL-500 full-load setting



The figure 1.16 shows that when it is full-load mode, the RMS values of Vo-AB, Vo-BC and Vo-CA are 1.12V (39.024V in actual

value), 1.11V (38.676V in actual value) and 1.12V (39.024V in actual value), respectively, and the RMS value of Io-A is 1.08A (2.265A in actual value).

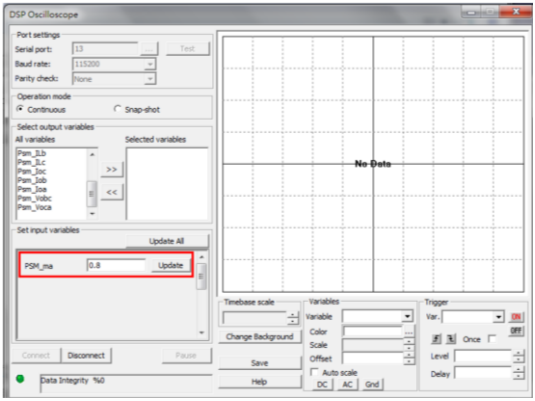
Figure 1.16 Full-load measured waveform



(4) Duty Change

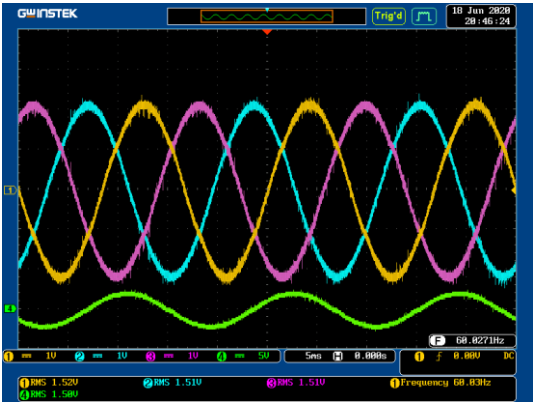
The figure 1.17 shows that the Duty parameter in circuit, which experienced the PSM_ma of "Set input variables" adjusted by RS232, is altered from default 0.6 to 0.8. Please press the Update.

Figure 1.17 PSIM DSP oscilloscope command value setting



The figure 1.18 shows that when DSO oscilloscope command value is adjusted from 0.6 to 0.8, the RMS values of Vo-AB, Vo-BC and Vo-CA are 1.52V (52.692V in actual value), 1.51V (52.613V in actual value) and 1.51V (52.613V in actual value), respectively, and the RMS value of Io-A is 1.50A (3.146A in actual value).

Figure 1.18 DSP oscilloscope command value is 0.8



After experiment, power off PEK-530→PSW160-7.2→PEK-005A→ GPL-500 in order properly.

Per differed test conditions, fill in the table 1.1 and 1.2 with the measured values of V_O and I_O in order. Also refer to the table 0.1 for the sensing ratio followed by filling in with actual values.

Table 1.1 Output voltage current measured data in varied settings of GPL-500

GPL-500	Vo-AB(Vrms) (Measured value)	Vo-AB(Vrms) (Actual value)	Vo-BC(Vrms) (Measured value)	Vo-BC(Vrms) (Actual value)
No load	1.22V	42.509V	1.21V	42.16V
Half load	1.13V	39.373V	1.13V	39.373V
Full load	1.12V	39.024V	1.11V	38.676V

GPL-500	Vo-CA(Vrms) (Measured value)	Vo-CA(Vrms) (Actual value)	Io-A(Irms) (Measured value)	Io-A(Irms) (Actual value)
No load	1.22V	42.509V	0.147A	0.308A
Half load	1.13V	39.373V	0.567A	1.189A
Full load	1.12V	39.024V	1.08A	2.265A

Table 1.2 Output voltage current measured data in varied Duties

Duty Commad value	Vo-AB(Vrms) (Measured value)	Vo-AB(Vrms) (Actual value)	Vo-BC(Vrms) (Measured value)	Vo-BC(Vrms) (Actual value)
0.6	1.12V	39.024V	1.11V	38.676V
0.8	1.52V	52.962V	1.51V	52.613V

Duty Commad value	Vo-CA(Vrms) (Measured value)	Vo-CA(Vrms) (Actual value)	Io-A(Irms) (Measured value)	Io-A(Irms) (Actual value)
0.6	1.12V	39.024V	1.08A	2.265A
0.8	1.51V	52.613V	1.50A	3.146A

The Conclusion

This experiment is the open loop system. It has seen that, from no load to full load within the table 1.1, output current is increasing gradually and output voltage is dropping in accord with load changes. From the table 1.2, it has seen that output voltage fluctuates in accordance with Duty changes.

Experiment 2 – Three Phase Stand-alone inverter

Circuit Simulation

Inverter Specification

DC Voltage V_{DC} = 100V

F_s = 18kHz，V_{tri} = $10V_{pp}$ (PWM)

C_d = 330uF，L = 1mH，C = 10uF

K_s = 0.3 (AC current sensing factor)

K_v = 1/60 (DC voltage sensing factor)

K_v = 1/40 (DC voltage sensing factor)

The analogue circuit diagram based on the parameters above is as the following figure 2.1 shown:
PSIM File: PEK-530_Sim2_3P_SA_Inv(60Hz)_V11.1.5_V1.1

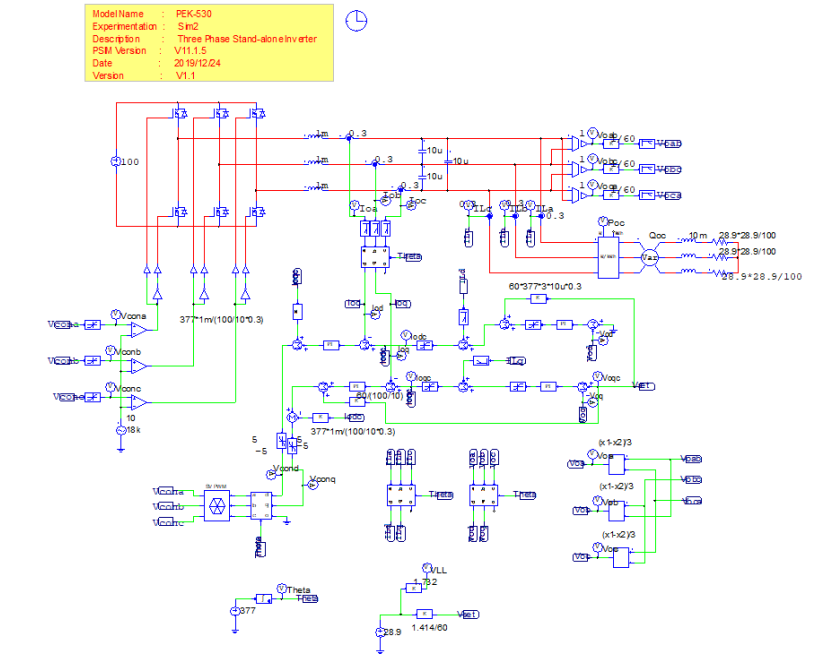


Figure 2.1 Experiment 2 PSIM analogue circuit diagram

The simulation results are shown within the figure 2.2 and 2.3:

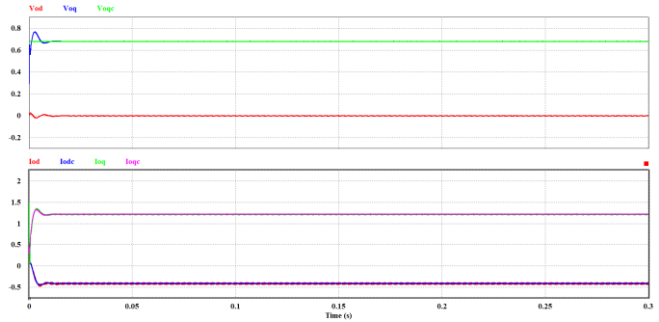


Figure 2.2 Experiment 2 analogue circuit simulation waveforms

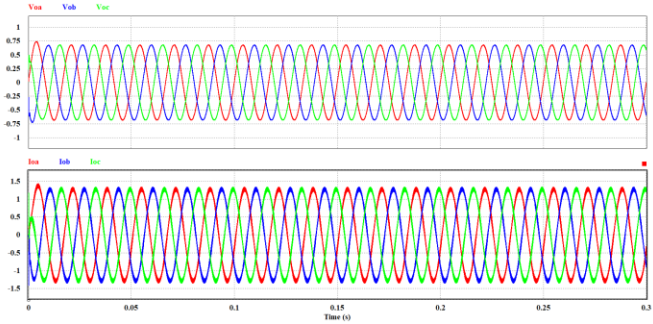


Figure 2.3 Experiment 2 analogue circuit simulation waveforms

The digital circuit diagram based on the analogue circuit is shown as the figure 2.4:

PSIM File: PEK-530_Lab2_3P_SA_Inv(60Hz)_V11.1.5_V1.1

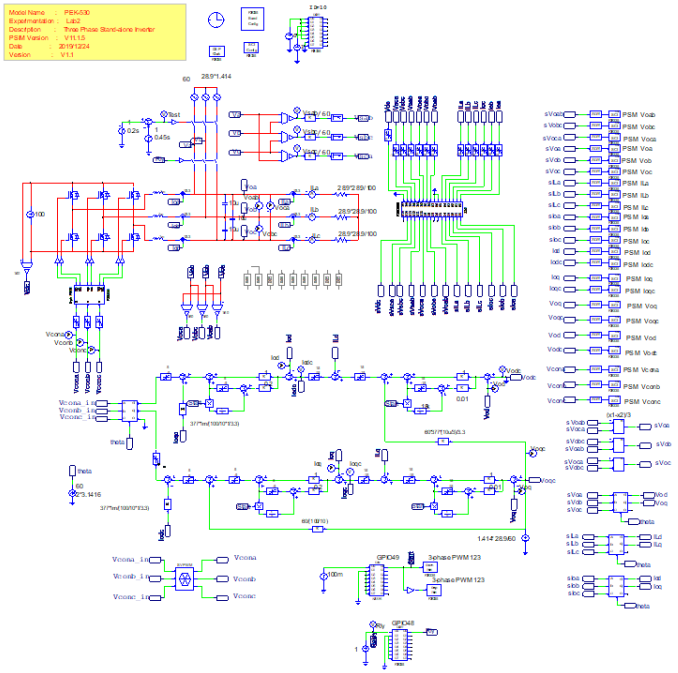


Figure 2.4 Experiment 2 PSIM analogue circuit diagram

The simulation results are shown within the figure 2.5 and 2.6:

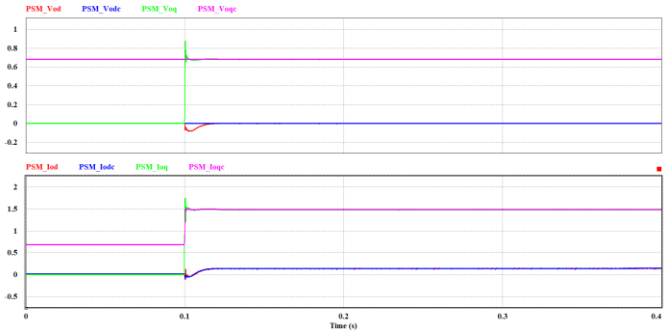


Figure 2.5 Experiment 2 digital circuit simulation waveforms

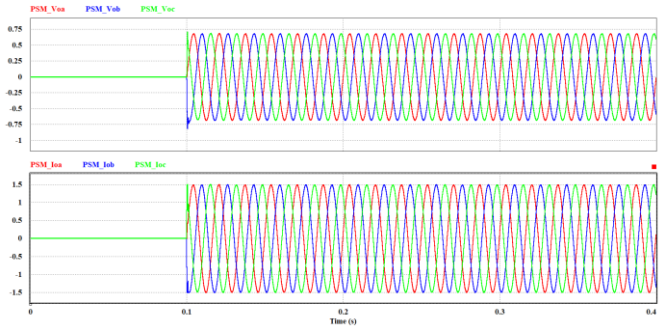


Figure 2.6 Experiment 2 digital circuit simulation waveforms

After confirming simulation, the corresponding C Code will be generated automatically via "Generate Code" of "Simulate".

Experiment Devices

The required devices for experiment are as follows. Refer to user manuals of each device before operation:

- PEK-530 * 1
- PEK-005A * 1
- PEK-006 * 1
- PTS-5000 * 1 (with GDS-2204E, PSW160-7.2 and GPL-500)
- PC * 1

Experiment Procedure

1. The experiment wiring is shown as the figure 2.7. Please follow it to complete wiring.

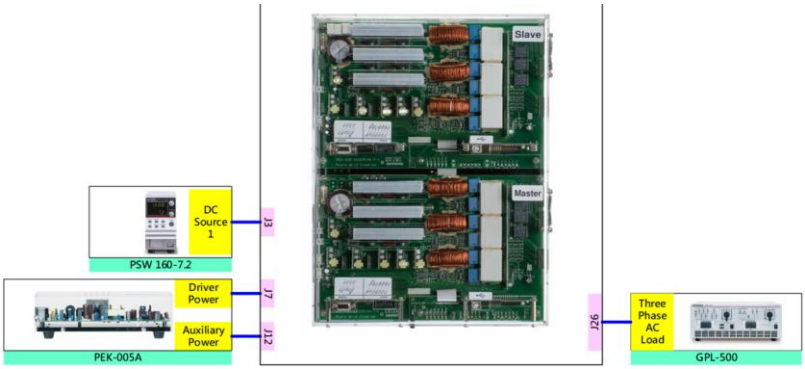


Figure 2.7 Experiment 2 wiring figure

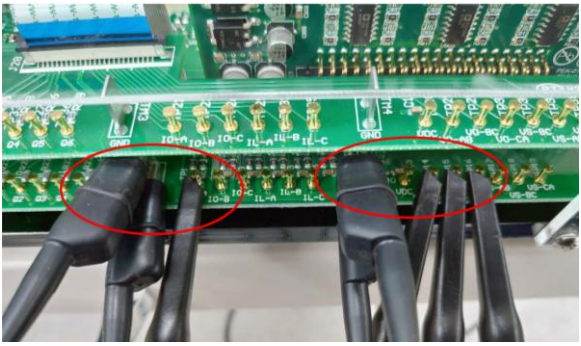
2. After wiring, make sure the PEK-530 switch is OFF followed by turning the PEK-005A switch ON. The DSP red indicator lights on as the figure 2.8 shown, which means the DSP power is steadily normal.

Figure 2.8 DSP normal status with light on

3. Refer to the appendix B for burning procedure.

4. Connect the test leads of oscilloscope to Vo-AB, Vo-BC and Vo-CA, respectively, followed by connecting GND of probe to the GND terminal as the figure 1.9 shown.

Figure 2.9
Oscilloscope test leads wiring

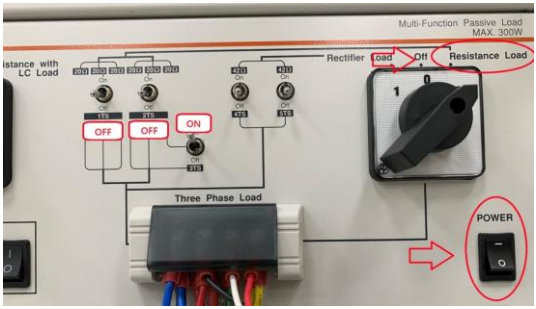


5. Refer to the figure 2.10 for the operation steps of PSW160-7.2. Power on PSW160-7.2→Click on Set key followed by adjusting voltage to 100V via voltage knob and adjusting current to 3A via current knob.

Figure 2.10
The settings of PSW

6. As the figure 2.11 shown, follow the steps below for GPL-500 operation. Power on GPL-500 → Rotate the Three Phase Lord knob to 2 (Resistance Load) → Set 1TS and 2TS as OFF, and 3TS as ON, which indicates no-load mode.

Figure 2.11
The no-load setting of GPL-500



7. After setting up and turning on PSW power output, finally turn on the switch of PEK-530

The purpose of experiment

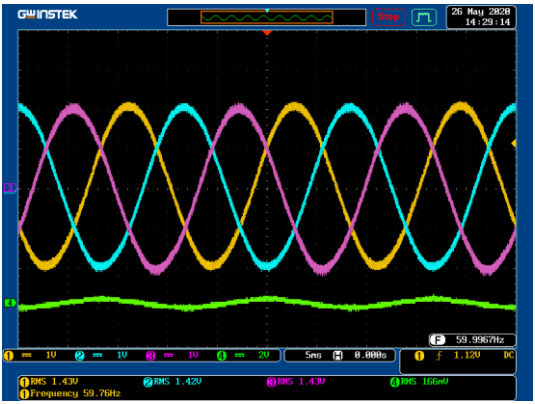
This experiment, which involves three phase inverter, ensures that output voltage, via close-loop control, maintains stable output with balanced state under load fluctuations. Also it observes load current state.

The experiment result

(1) No Load

The figure 2.12 shows that when it is no-load mode, the RMS values of Vo-AB, Vo-BC and Vo-CA are 1.43V (49.826V in actual value), 1.42V (49.477V in actual value) and 1.43V (49.826V in actual value), respectively, and the RMS value of Io-A is 0.166A (0.348A in actual value).

Figure 2.12 No-load measured waveform



(2) Half Load (20Ω)

The figure 21.13 shows that 1Ts and 3TS of GPL-500 are set ON, whereas 2TS is set OFF, which indicates half load.

The figure 2.14 shows that when it is hald-load mode, the RMS value of Vo-AB, Vo-BC and Vo-CA is 1.42V (49.477V in actual value), 1.41V (49.129V in actual value) and 1.43V (49.826V in actual value), respectively, and the RMS value of Io-A is 0.711A (1.491A in actual value).

Figure 2.13 GPL-500 half-load setting

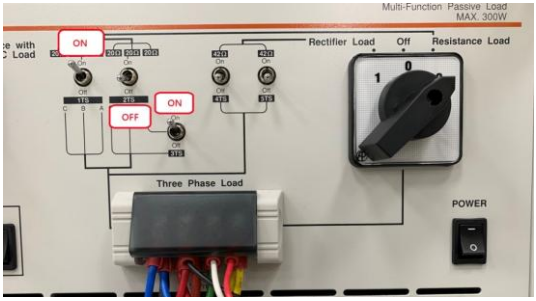
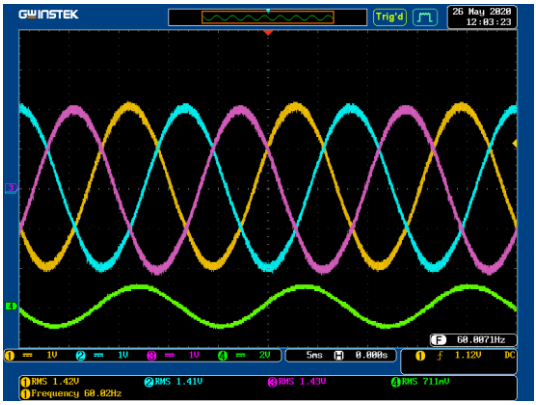


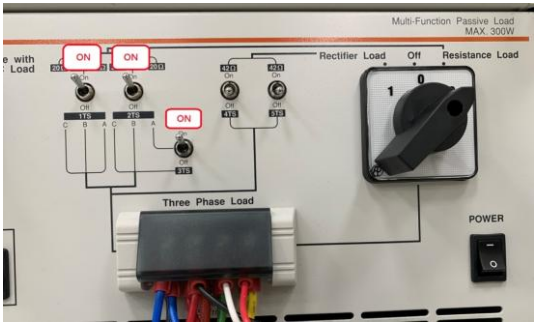
Figure 2.14 Half-load measured waveform



(3) Full Load (10Ω)

The figure 2.15 shows that 1Ts, 2Ts and 3TS of GPL-500 are set ON, which indicates full load.

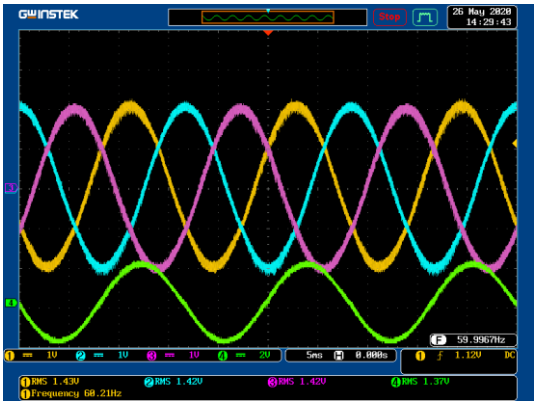
Figure 2.15 GPL-500 full-load setting



The figure 2.16 shows that when it is full-load mode, the RMS value of Vo-AB, Vo-BC and Vo-CA is 1.43V (49.826V in actual value), 1.42V (49.477V in actual value) and 1.42V (49.477V in actual value), respectively, and the RMS value of Io-A is 1.37A (2.873A in actual value).

The figure 2.16 shows that when it is full-load mode, the RMS values of Vo-AB, Vo-BC and Vo-CA are 1.43V (49.826V in actual value), 1.42V (49.477V in actual value) and 1.42V (49.477V in actual value), respectively, and the RMS value of Io-A is 1.37A (2.265A in actual value).

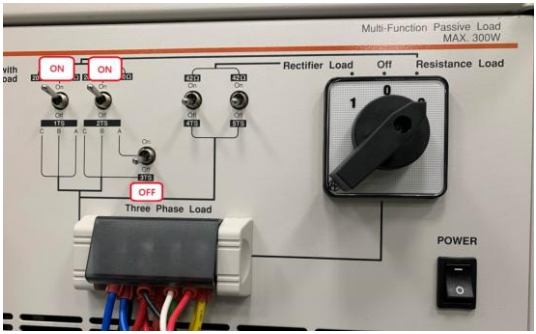
Figure 2.16 Full-load measured waveform



(4) Unbalanced Load (A phase 20Ω, B and C phase 10Ω)

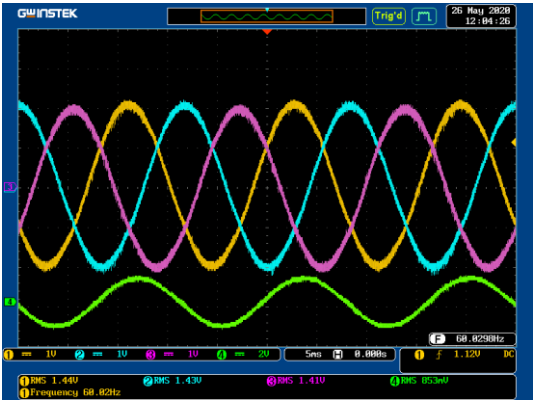
The figure 2.17 shows that 1Ts and 2TS of GPL-500 are set ON, whereas 3TS is set OFF, which indicates unbalanced load.

Figure 2.17 GPL-500 unbalanced-load setting



The figure 2.18 shows that when it is unbalanced load, the RMS value of Vo-AB, Vo-BC and Vo-CA are 1.44V (50.174V in actual value), 1.43V (49.826V in actual value) and 1.41V (49.129V in actual value), respectively, and the three phase voltage remains balanced state.

Figure 2.18 Unbalanced-load Vo measured waveform

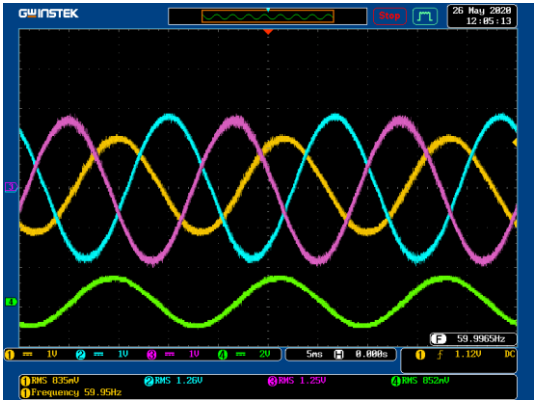


As the figure 2.19 shown, connect the test leads of oscilloscope to IL-A, IL-B and IL-C for observation.

Figure 2.19 Oscilloscope test leads wiring

The figure 2.20 shows that when it is unbalanced load, the RMS values of IL-A, IL-B and IL-C are 0.835A (1.751A in actual value), 1.26A (2.643A in actual value) and 1.25A (2.622A in actual value), respectively, and the three load current is under unbalanced-load state.

Figure 2.20 Unbalanced-load IL measured waveform



After experiment, power off PEK-530→PSW160-7.2→PEK-005A→ GPL-500 in order properly.

Per no load, half load, full load and unbalanced load settings of GPL-500, fill in the table 2.1 and 2.2 with the measured values of V_O, I_O and IL in order. Also refer to the table 0.1 for the sensing ratio followed by filling in with actual values.

Table 2.1 Output voltage current measured data in varied settings of GPL-500

GPL-500	Vo-AB(Vrms) (Measured value)	Vo-AB(Vrms) (Actual value)	Vo-BC(Vrms) (Measured value)	Vo-BC(Vrms) (Actual value)
No load	1.43V	49.826V	1.42V	49.477V
Half load	1.42V	49.477V	1.41V	49.129V
Full load	1.43V	49.826V	1.42V	49.477V
Unbalanced load	1.44V	50.174V	1.43V	49.826V

GPL-500	Vo-CA(Vrms) (Measured value)	Vo-CA(Vrms) (Actual value)	Io-A(Irms) (Measured value)	Io-A(Irms) (Actual value)
No load	1.43V	49.826V	0.166A	0.348A
Half load	1.43V	49.826V	0.711A	1.482A

Full load	1.42V	49.477V	1.37A	2.873A
Unbalanced load	1.41V	49.129V		

Table 2.2 Load current measured data in unbalanced load of GPL-500

GPL-500	IL-A(Vrms) (Measured value)	IL-A(Vrms) (Actual value)	IL-B(Vrms) (Measured value)	IL-B(Vrms) (Actual value)	IL-C(Vrms) (Measured value)	IL-C(Vrms) (Actual value)
Unbalanced load	0.835A	1.751A	1.26A	2.643A	1.25A	2.622A

The conclusion

This experiment, which involves three phase inverter system, ensures that three phase output voltage, from duration of no load through full load, maintains stable output with balanced state and gradual three phase output current increment. When switching to unbalanced load, the load current is unbalanced-load state though, three phase output voltage keeps balanced state still.

Experiment 3 – Three Phase Grid-connected Inverter

Circuit Simulation

Inverter Specification

DC Voltage V_{DC} = 100V

AC Source Voltage V_{LL} = 50V_{rms}

F_s = 18kHz，V_{tri} = 10V_{pp} (PWM)

C_d = 330uF，L = 1mH，C = 10uF

K_s = 0.3 (AC current sensing factor)

K_v = 1/60 (DC voltage sensing factor)

K_v = 1/40 (DC voltage sensing factor)

The analogue circuit diagram based on the parameters above is as the following figure 3.1 shown:
PSIM File: PEK-530_Sim3_3P_GC_Inv(60Hz)_V11.1.5_V1.1

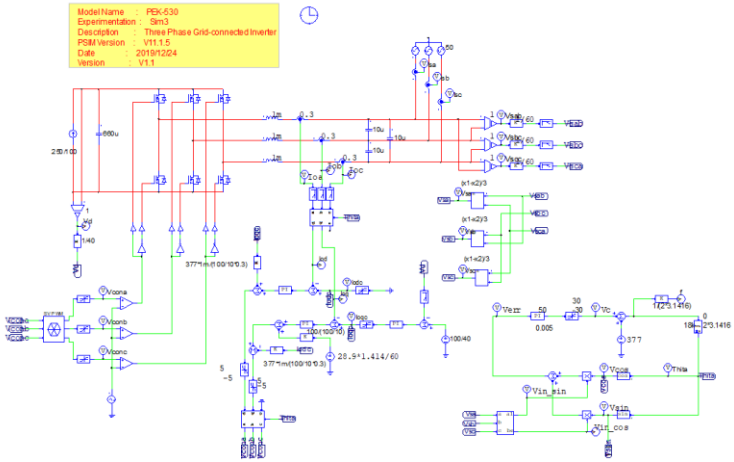


Figure 3.1 Experiment 3 PSIM analogue circuit diagram

The simulation results are shown within the figure 3.2 and 3.3:

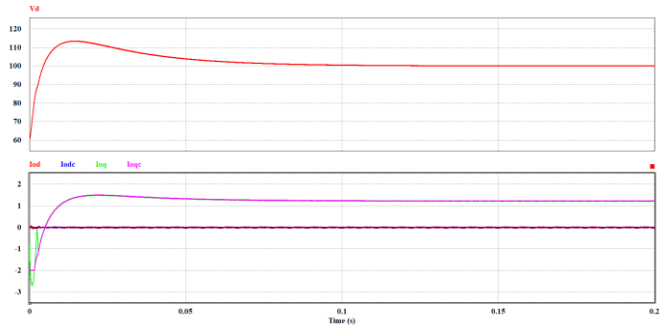


Figure 3.2 Experiment 3 analogue circuit simulation waveforms

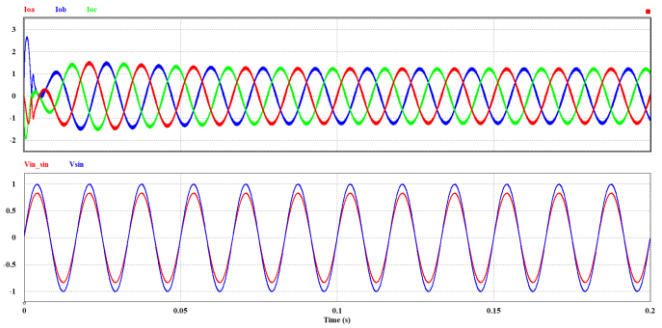


Figure 3.3 Experiment 3 analogue circuit simulation waveforms

The digital circuit diagram based on the analogue circuit is shown as the figure 3.4:
PSIM File: PEK-530_Lab3_3P_GC_Inv(60Hz)_V11.1.5_V1.1

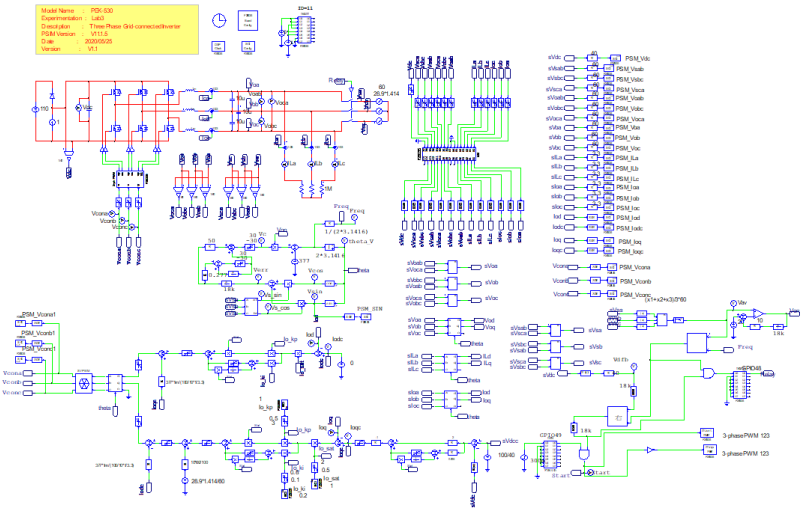


Figure 3.4 Experiment 3 PSIM digital circuit diagram

The simulation result is shown within the figure 3.5:

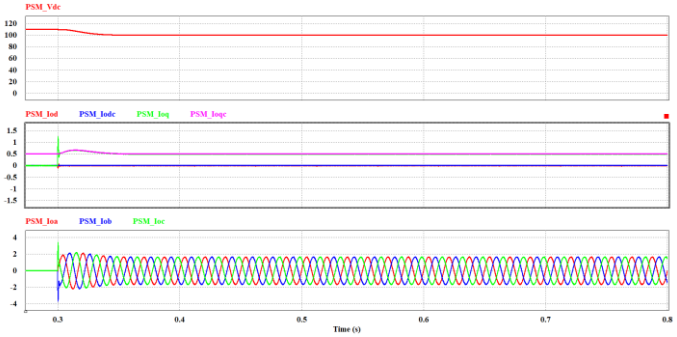


Figure 3.5 Experiment 3 digital circuit simulation waveforms

After confirming simulation, the corresponding C Code will be generated automatically via “Generate Code” of “Simulate”.

Experiment Devices

The required devices for experiment are as follows. Refer to user manuals of each device before operation:

- PEK-530 * 1
- PEK-005A * 1
- PEK-006 * 1
- PTS-5000 * 1 (with GDS-2204E, PSW160-7.2, APS-300 and GPL-500)
- PC * 1

Experiment Procedure

1. The experiment wiring is shown as the figure 3.6. Please follow it to complete wiring.

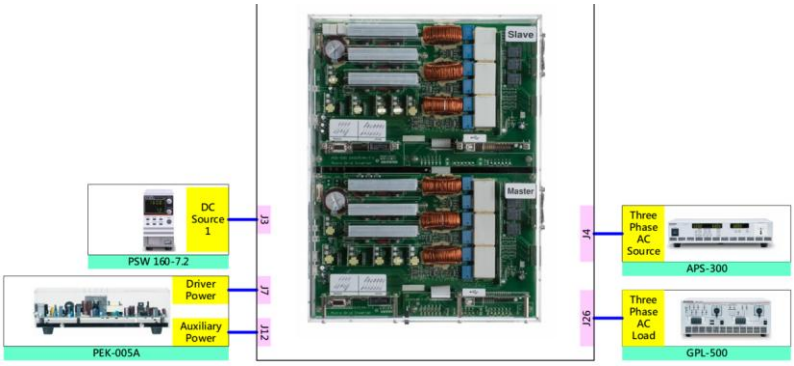


Figure 3.6 Experiment 3 wiring figure

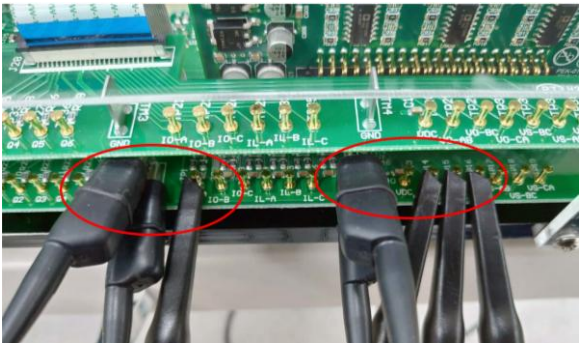
2. After wiring, make sure the PEK-530 switch is OFF followed by turning the PEK-005A switch ON. The DSP red indicator lights on as the figure 3.7 shown, which means the DSP power is steadily normal.

Figure 3.7 DSP normal status with light on

3. Refer to the appendix B for burning procedure.

4. Connect the test leads of oscilloscope to Vo-AB, Vo-BC and Vo-CA, respectively, followed by connecting GND of probe to the GND terminal. The measurement point of terminal is the common ground.

Figure 3.8
Oscilloscope test leads wiring



5. Refer to the figure 3.9 for the operation steps of PSW160-7.2. Power on PSW160-7.2→Click on Set key followed by adjusting voltage to 100V via voltage knob and adjusting current to 1A via current knob.

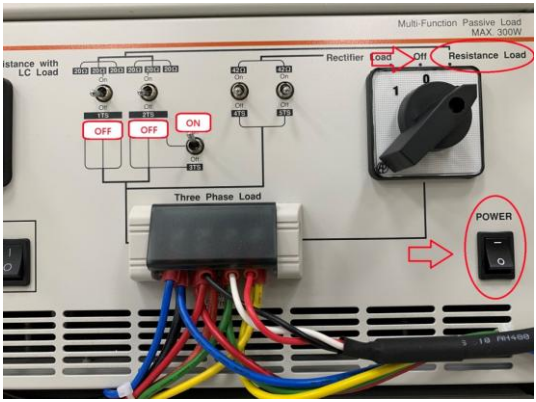
Figure 3.9
The settings of PSW

6. As the figure 3.10 shown, follow the steps below for APS-300 operation. Power on APS-300 → Set frequency as 60Hz → Set operation mode as 3P4W → Set voltage as 28.86V.

Figure 3.10
The settings of APS-300

7. As the figure 3.11 shown, follow the steps below for GPL-500 operation. Power on GPL-500 → Rotate the Three Phase Lord knob to 2 (Resistance Load) → Set 1TS and 2TS as OFF, and 3TS as ON, which indicates no-load mode.

Figure 3.11
The no-load setting of GPL-500



8. After setting up and turning on PSW and APS-300 power output, finally turn on the switch of PEK-530.

The purpose of experiment

This experiment, which involves three phase grid-connected inverter, discusses power changes between inverter and power grid under the conditions of different load power.

The experiment result

Because direction of conductance current is positive under boost mode, the current will be negative observed from oscilloscope while operating under buck mode.

(1) No Load

The figure 3.12 indicates measured waveforms of three phase voltage output Vo-AB, Vo-BC and Vo-CA.

The figure 3.13 shows that PSW output power is 99.86W. When it is no-load mode, the power generated by inverter is absorbed by APS-300. Therefore, it has seen that the power displayed on APS-300 is single phase -31.6W and thus three phase total power is -31.6W*3= −94.8W (minus sign indicates absorbed power).

Figure 3.12 Vo measured waveform

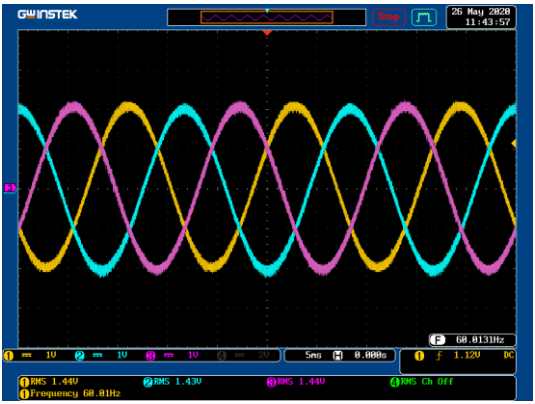
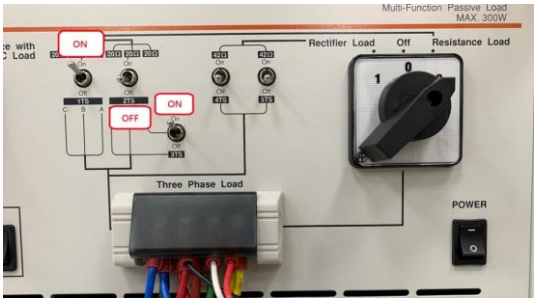


Figure 3.13
PSW and APS-300 power state when no load

(2) Half Load (20Ω)

Set 1TS and 3TS as ON, and 2TS as OFF, which indicates half load as the figure 3.14 shown.

Figure 3.14 The half-load setting of GPL-500



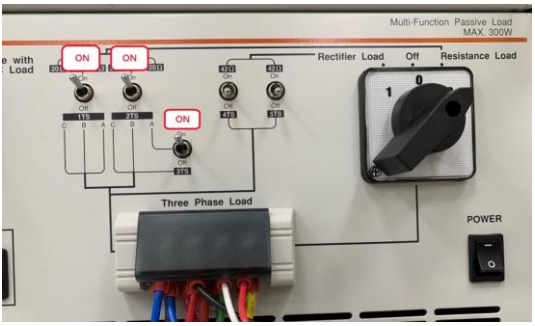
The figure 3.15 shows that when it is half-load mode, PSW output power is 99.88W and the power consumed by load is increasing up to 125W. Therefore, PSW output power is not able to meet the requirement of load. Because APS-300 needs to provide 25W for maintaining system power balance, it has seen that APS-300 power is single phase 10.1W and three phase total power is 10.1W*3=30.3W.

Figure 3.15
PSW and APS-300 power state under half load

(3) Full Load (10Ω)

Set 1TS, 2TS and 3TS as ON, which indicates full load as the figure 3.16 shown.

Figure 3.16 The full-load setting of GPL-500



The figure 3.17 shows that when it is full-load mode, PSW output power is 99.85W and the power consumed by load is increasing up to 250W. Therefore, PSW output power is not able to meet the requirement of load. Because APS-300 needs to provide 150W for maintaining system power balance, it has seen that APS-300 power is single phase 50.6W and three phase total power is 50.6W*3=151.8W.

Figure 3.17 PSW and APS-300 power state under full load

After experiment, power off PEK-530→PSW160-7.2→PEK-005A→ GPL-500 in order properly.

Fill in the table 3.1 with the power of PSW and APS-300 under vaired loads.

Table 3.1 Power state of PSW and APS-300 under varied loads

Load Power	PSW Output Power	APS Output Power	
No Load (0W)	99.86W	-94.8W	99.86 + (-94.8) ≒ 0

Mid Load (125W)	99.88W	30.3W	99.88 +30.3 ≒ 125
Full Load (250W)	99.85W	151.8W	99.85 +151.8 ≒ 250

The conclusion

This experiment is the grid-connected three phase inverter system. When power provided by inverter is greater than requirement of load, the remaining power will be feedbacked to power grid. By contrast, when power provided by inverter can not afford to support power consumed by load, power grid will then output power to compensate the requirement of load so that system power balance is farily maintained.

Experiment 4 – PQ Control of Three-phase Grid-connected inverter

Circuit Simulation

Inverter Specification

DC Voltage V_{DC} = 100V

AC Source Voltage V_{LL} = 50V_{rms}

F_s = 18kHz，V_{tri} = 10V_{pp} (PWM)

C_d = 330uF，L = 1mH，C = 10uF

K_s = 0.3 (AC current sensing factor)

K_v = 1/60 (DC voltage sensing factor)

K_v = 1/40 (DC voltage sensing factor)

The analogue circuit diagram based on the parameters above is as the following figure 4.1 shown:
PSIM File: PEK-530_Sim4_3P_GC_Inv_PQ(60Hz)_V11.1.5_V1.1

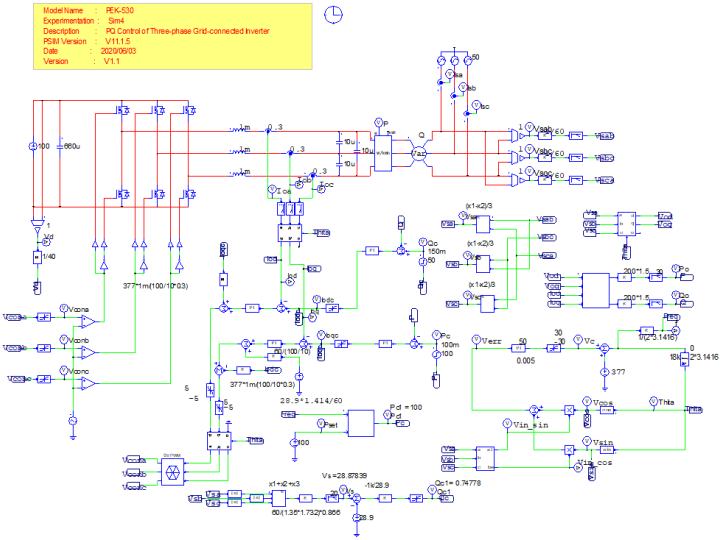


Figure 4.1 Experiment 4 PSIM analogue circuit diagram

The simulating result is shown as the figure 4.2:

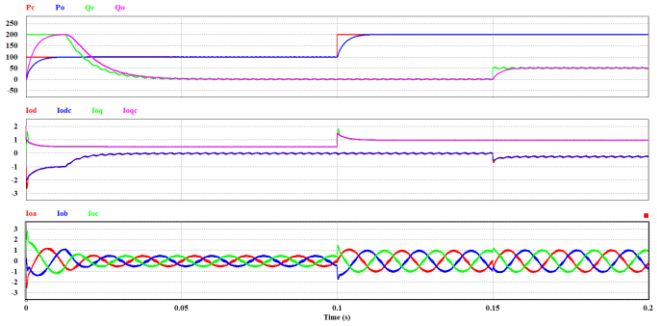


Figure 4.2 Experiment 4 analogue circuit simulation waveform

The digital circuit diagram based on the analogue circuit is shown as the figure 4.3:
PSIM File: PEK-530_Lab4_3P_GC_Inv_PQ(60Hz)_V11.1.5_V1.1

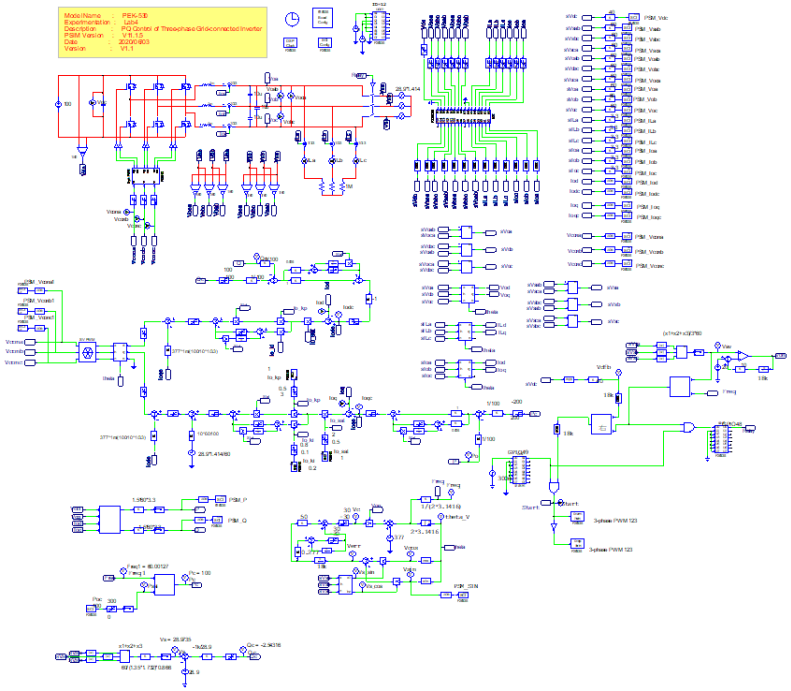


Figure 4.3 Experiment 4 PSIM digital circuit diagram

The simulating results are shown as the figure 4.4 and 4.5:

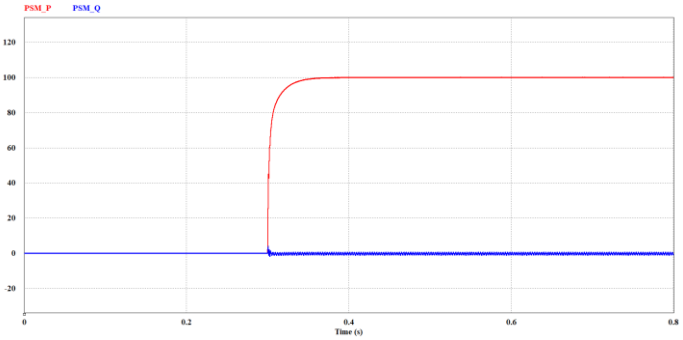


Figure 4.4 Experiment 4 digital circuit simulation waveform

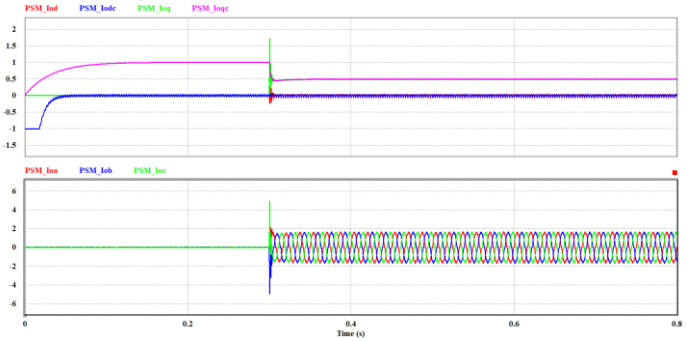


Figure 4.5 Experiment 4 digital circuit simulation waveform

After confirming simulation, the corresponding C Code will be generated automatically via “Generate Code” of “Simulate”.

Experiment Devices

The required devices for experiment are as follows. Refer to user manuals of each device before operation:

- PEK-530 * 1
- PEK-005A * 1
- PEK-006 * 1
- PTS-5000 * 1 (with GDS-2204E, PSW160-7.2, APS-300 and GPL-500)
- PC * 1

Experiment Procedure

1. The experiment wiring is shown as the figure 4.6. Please follow it to complete wiring.

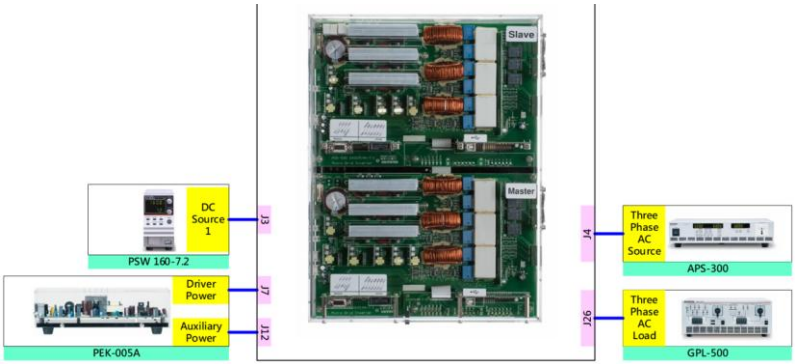


Figure 4.6 Experiment 5 wiring figure

2. After wiring, make sure the PEK-530 switch is OFF followed by turning the PEK-005A switch ON. The DSP red indicator lights on as the figure 4.7 shown, which means the DSP power is steadily normal.

Figure 4.7 DSP normal status with light on

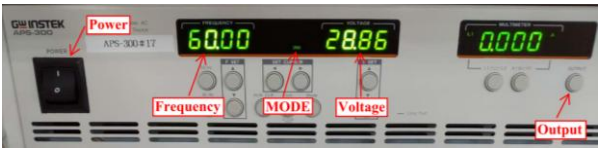
3. Refer to the appendix B for burning procedure followed by the appendix C for RS232 connection.

4. Refer to the figure 4.8 for the operation steps of PSW160-7.2. Power on PSW160-7.2→Click on Set key followed by adjusting voltage to 100V via voltage knob and adjusting current to 2A via current knob.

Figure 4.8
The settings of PSW

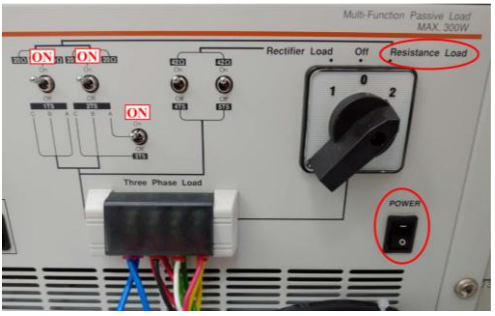
5. As the figure 4.9 shown, follow the steps below for APS-300 operation. Power on APS-300 → Set frequency as 60Hz → Set operation mode as 3P4W → Set voltage as 28.86V.

Figure 4.9
The settings of PSW



6. As the figure 4.10 shown, follow the steps below for GPL-500 operation. Power on GPL-500 → Rotate the Three Phase Lord knob to 2 (Resistance Load) → Set 1TS, 2TS and 3TS as ON, which indicates full-load mode.

Figure 4.10
The full-load setting of GPL-500



7. After setting up and turning on PSW and APS-300 power output, finally turn on the switch of PEK-530.

The purpose of experiment

This experiment is application of smart inverter. When voltage or frequency change occurs within grid power, the inverter will adjust power (active or reactive) output via system PQ controller in accord with the latest condition.

The experiment result

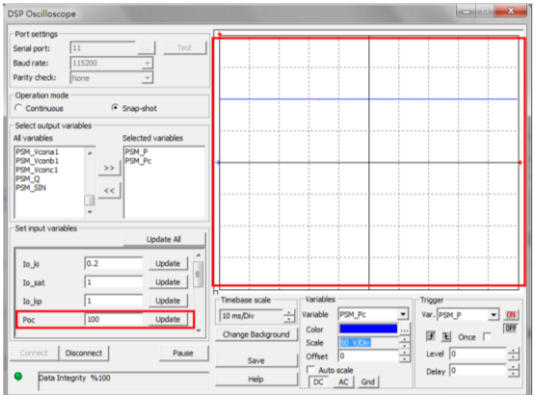
1. Active Power Control (P-ω)

(1) Frequency 60Hz

As the figure 4.11 and 4.12 shown, when frequency of APS-300 is set 60Hz, the active power command value, PSM_Poc, will be set 100 and 100W will be displayed on DSP oscilloscope.

Figure 4.11 APS-300 set frequency 60Hz

Figure 4.12 Active power waveform of APS-300 set frequency 60Hz displayed on DSP oscilloscope

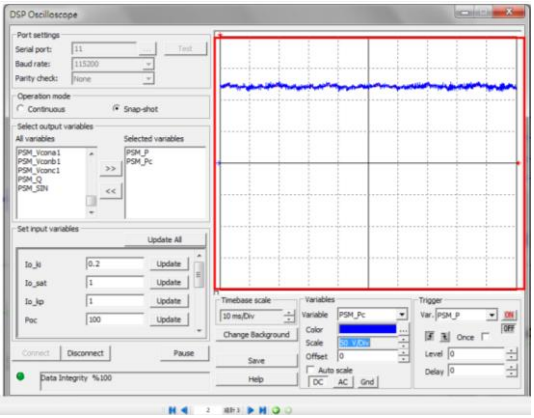


(2) Frequency 59.3Hz

As the figure 4.13 and 4.14 shown, when frequency of APS-300 is set 59.3Hz, the power displayed on DSP oscilloscope is raising.

Figure 4.13
APS-300 set frequency 59.3Hz

Figure 4.14
Active power waveform of APS-300 set frequency 59.3Hz displayed on DSP oscilloscope

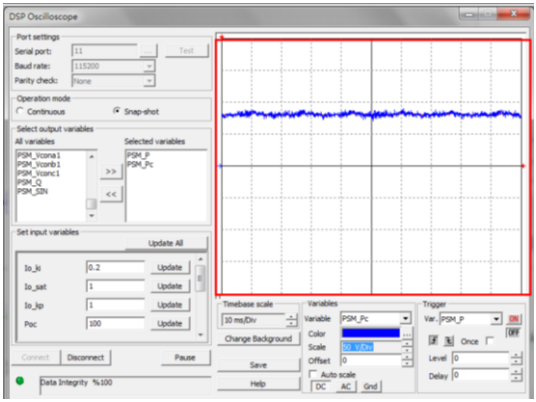


(3) Frequency 60.7Hz

As the figure 4.15 and 4.16 shown, when frequency of APS-300 is set 60.7Hz, the power displayed on DSP oscilloscope is dropping.

Figure 4.15
APS-300 set frequency 60.7Hz

Figure 4.16 Active power waveform of APS-300 set frequency 60.7Hz displayed on DSP oscilloscope



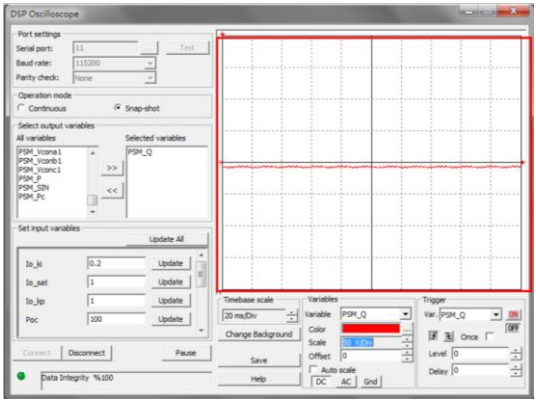
2. Reactive Power Control (Q-V)

(1) Voltage 28.86V

As the figure 4.17 and 4.18 shown, when voltage of APS-300 is set 28.86V, the reactive power waveform will be displayed on DSP oscilloscope.

Figure 4.17 APS-300 set voltage 28.86V

Figure 4.18 Reactive power waveform displayed on DSP oscilloscope when grid power voltage is 28.86V

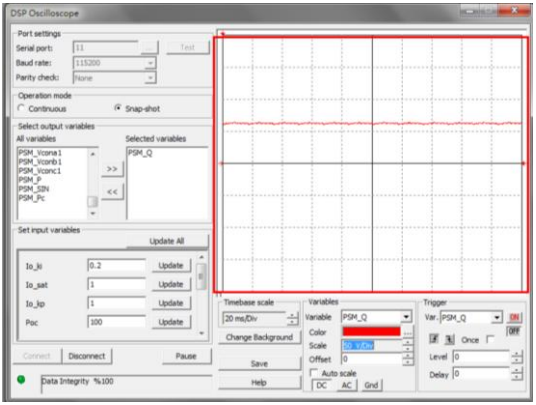


(2) Voltage 26.86V

As the figure 4.19 and 4.20 shown, when voltage of APS-300 is set 26.86V, the reactive power waveform will be displayed on DSP oscilloscope.

Figure 4.19 APS-300 set voltage 28.86V

Figure 4.20 Reactive power waveform displayed on DSP oscilloscope when grid power voltage is 26.86V



(3) Voltage 30.86V

As the figure 4.21 and 4.22 shown, when voltage of APS-300 is set 30.86V, the reactive power waveform will be displayed on DSP oscilloscope.

Figure 4.21 APS-300 set voltage 30.86V

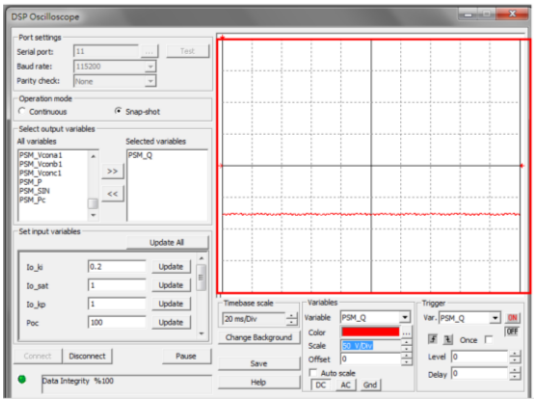


Figure 4.22 Reactive power waveform displayed on DSP oscilloscope when grid power voltage is 30.86V

The Conclusion

From the experiment, it is understandable that when frequency of grid power changes, inverter adjusts output power scale in accordance with frequency fluctuations. When, on the other hand, voltage of grid power changes, inverter adjusts output reactive power scale in light with voltage fluctuations.

Experiment 5 – P-ω and Q-V Droop control of Three Phase Stand-alone Inverter

Circuit Simulation

Inverter Specification	DC Voltage V_{DC} = 100V
	F_s = 18kHz，V_{tri} = 10V_{pp} (PWM)
	C_d = 330uF，L = 1mH，C = 10uF
	K_s = 0.3 (AC current sensing factor)
	K_v = 1/60 (DC voltage sensing factor)
	K_v = 1/40 (DC voltage sensing factor)

The analogue circuit diagram based on the parameters above is as the following figure 5.1 shown:
PSIM File: PEK-530_Sim5_3P_SA_Inv_PQ(60Hz)_V11.1.5_V1.1

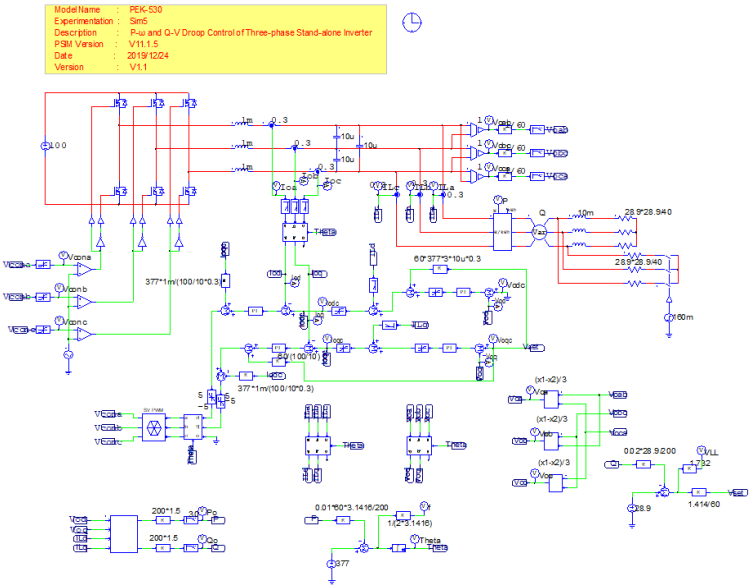


Figure 5.1 Experiment 5 PSIM analogue circuit diagram

The simulating results are shown as the figure 5.2 and 5.3:

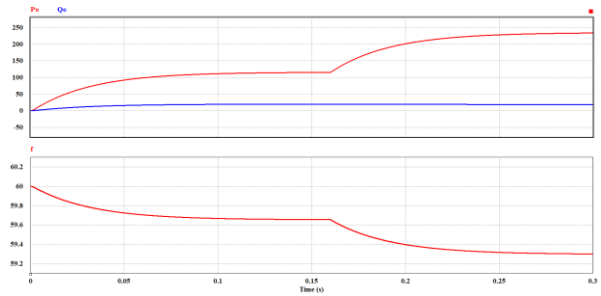


Figure 5.2 Experiment 5 analogue circuit simulation waveforms

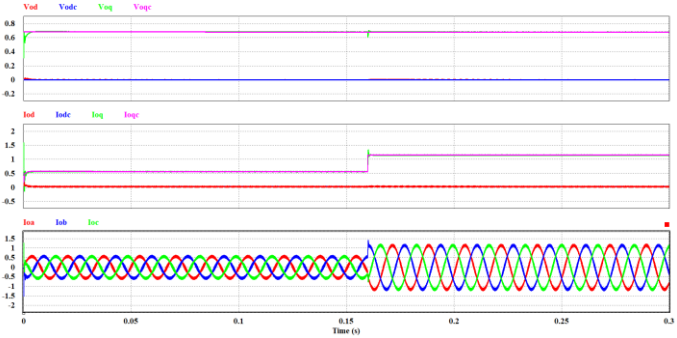


Figure 5.3 Experiment 5 analogue circuit simulation waveforms

The digital circuit diagram based on the analogue circuit is shown as the figure 5.4:

PSIM File: PEK-530_Lab5_3P_SA_Inv_PQ(60Hz)_V11.1.5_V1.1

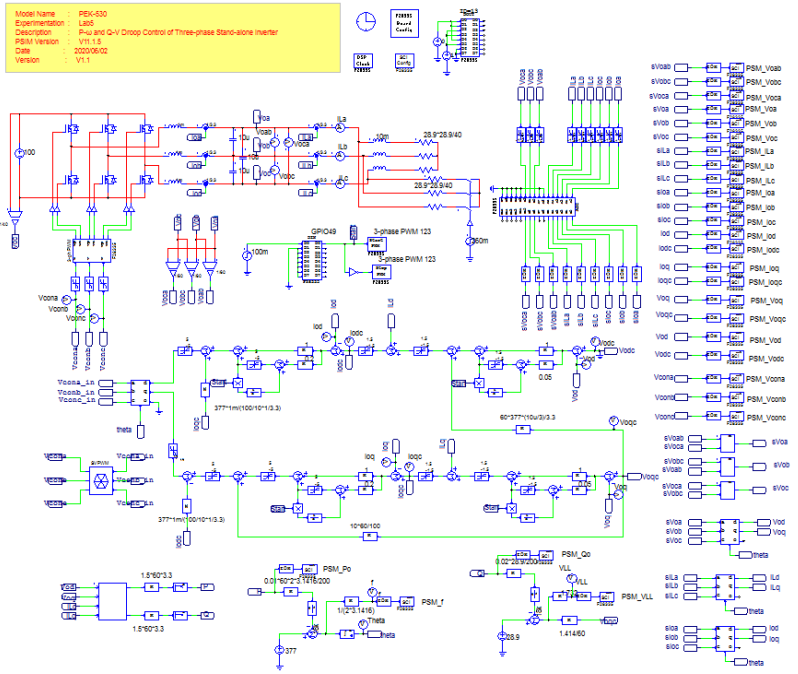


Figure 5.4 Experiment 5 PSIM digital circuit diagram

The simulating results are shown as the figure 5.5 and 5.6:

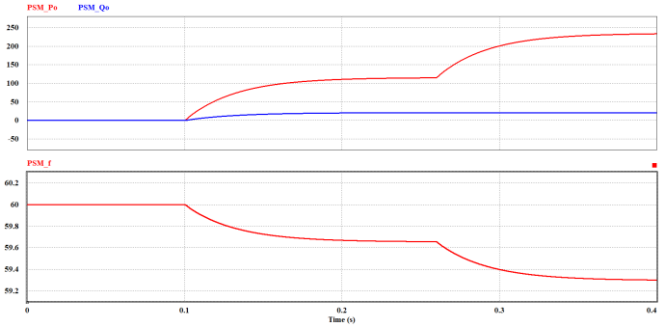


Figure 5.5 Experiment 5 digital circuit simulation waveforms

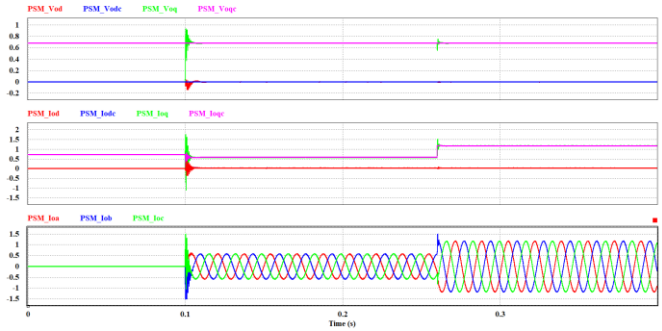


Figure 5.6 Experiment 5 digital circuit simulation waveforms

After confirming simulation, the corresponding C Code will be generated automatically via “Generate Code” of “Simulate”.

Experiment Devices

The required devices for experiment are as follows. Refer to user manuals of each device before operation:

- PEK-530 * 1
- PEK-005A * 1
- PEK-006 * 1
- PTS-5000 * 1 (with GDS-2204E, PSW160-7.2 and GPL-500)
- PC * 1

Experiment Procedure

1. The experiment wiring is shown as the figure 5.7. Please follow it to complete wiring.

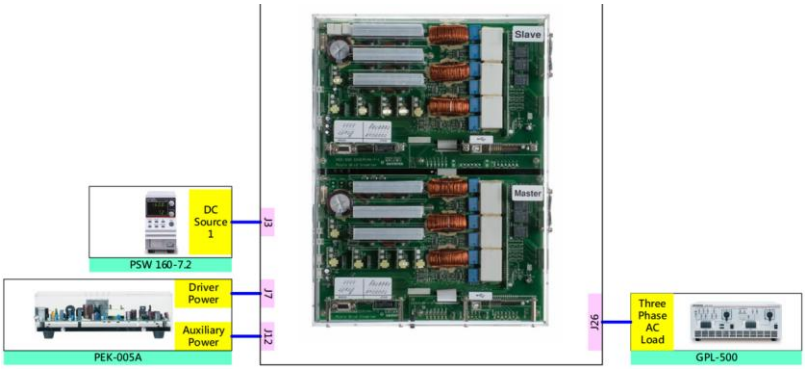


Figure 5.7 Experiment 1 wiring figure

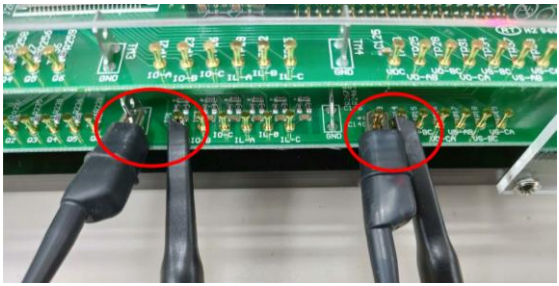
2. After wiring, make sure the PEK-530 switch is OFF followed by turning the PEK-005A switch ON. The DSP red indicator lights on as the figure 5.8 shown, which means the DSP power is steadily normal.

Figure 5.8 DSP normal status with light on

3. Refer to the appendix B for burning procedure followed by the appendix C for RS232 connection.

4. As the figure 5.9 shown, connect the test leads of oscilloscope to Vo-AB and Io-A, respectively, followed by connecting GND of probe to the GND terminal. The measurement point of terminal is the common ground.

Figure 5.9 Oscilloscope test leads wiring

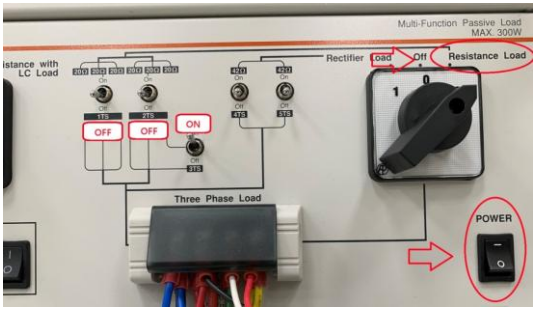


5. Refer to the figure 5.10 for the operation steps of PSW160-7.2. Power on PSW160-7.2→Click on Set key followed by adjusting voltage to 100V via voltage knob and adjusting current to 3A via current knob.

Figure 5.10 The settings of PSW

6. As the figure 5.11 shown, follow the steps below for GPL-500 operation. Power on GPL-500 → Rotate the Three Phase Lord knob to 2 (Resistance Load) → Set 1TS and 2TS as OFF, and 3TS as ON, which indicates no-load mode.

Figure 5.11 The no-load setting of GPL-500



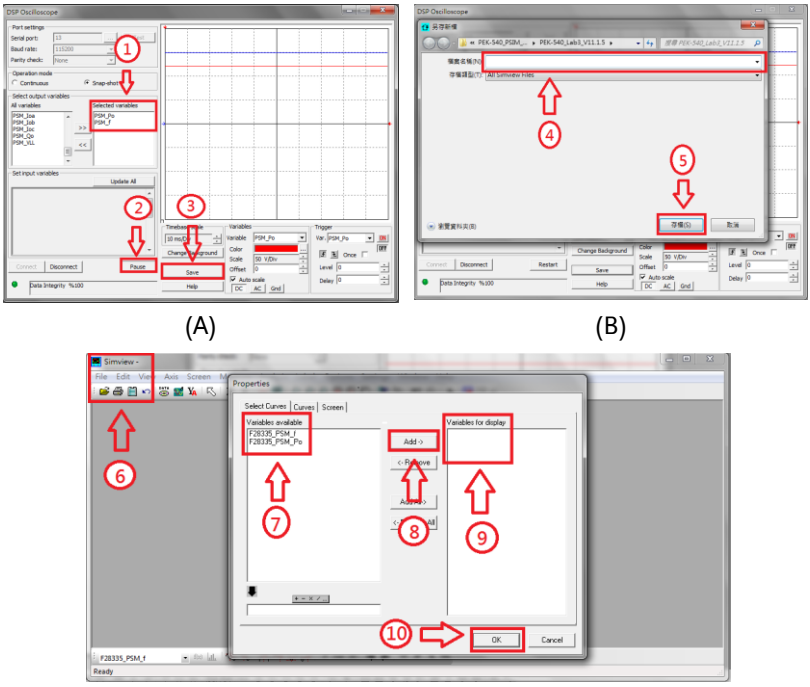
7. After setting up and turning on PSW power output, finally turn on the switch of PEK-530.

The purpose of experiment

This experiment is droop control applying to three phase inverter system. When active and reactive power change, we observe fluctuations from poutput voltage and frequency.

The experiment result

It is necessary to save the measured waveforms from DSP oscilloscope for carefully observation. The operation steps are shown as the figure 5.12. (1) select the required saved waveform →(2) click Pause key →(3) click Save key →(4) input filename →(4) save file →(6) open file via Simview →(7) select waveform to observe →(8) click Add →(9) the selected waveform will be shown on Variables for display →(10) click OK for observation.



(A) (B)

(C)

Figure 5.12 Operation steps of saving waveform on DSP oscilloscope

1. P-ω Control

(1) No Load

As the figure 5.13 and 5.14 shown, when it is no-load, it has seen that output frequency is 60Hz from both oscilloscope and DSP oscilloscope.

Figure 5.13 Oscilloscope measured waveform when no load

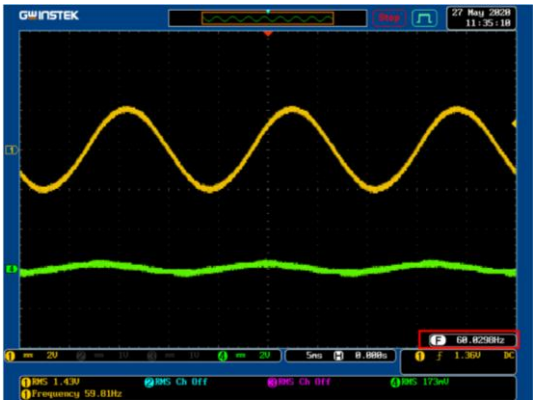
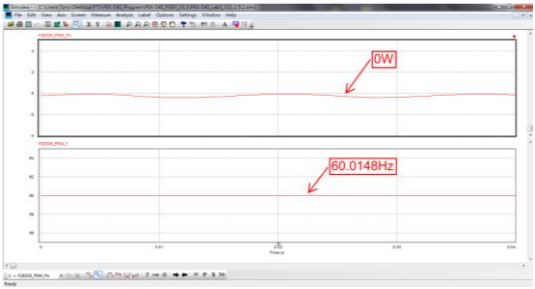


Figure 5.14 DSP oscilloscope measured waveform when no load



(2) Hald Load (20Ω)

The figure 5.15 shows that 1Ts and 3TS of GPL-500 are set ON, whereas 2TS is set OFF, which indicates half load.

As the figure 5.16 and 5.17 shown, when it is half-load, it has seen that output frequency is 59.6Hz from both oscilloscope and DSP oscilloscope.

Figure 5.15 GPL-500 half-load setting

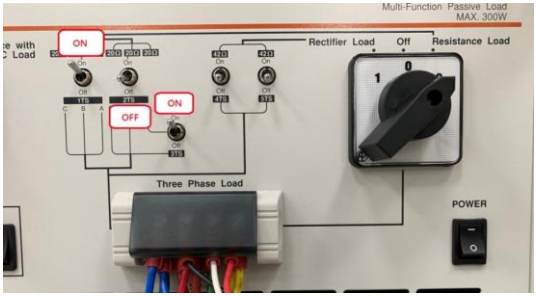


Figure 5.16 Oscilloscope measured waveform when half load

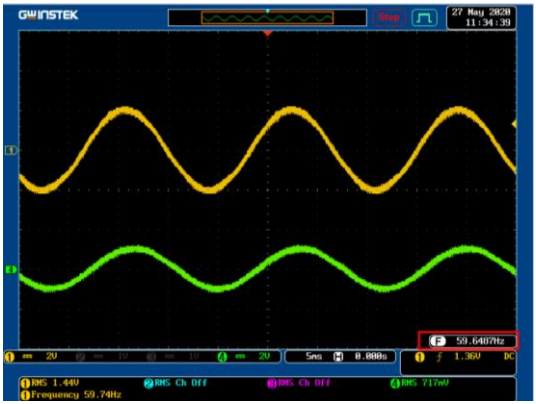
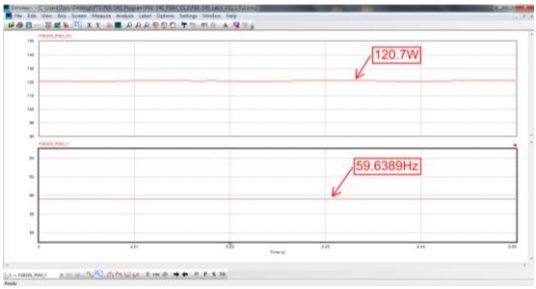


Figure 5.17 DSP oscilloscope measured waveform when half load



(3) Full Load (10Ω)

The figure 5.18 shows that 1Ts, 2Ts and 3TS of GPL-500 are set ON, which indicates full load.

As the figure 5.19 and 5.20 shown, when it is full-load, it has seen that output frequency is 59.2Hz from both oscilloscope and DSP oscilloscope.

Figure 5.18 GPL-500 full-load setting

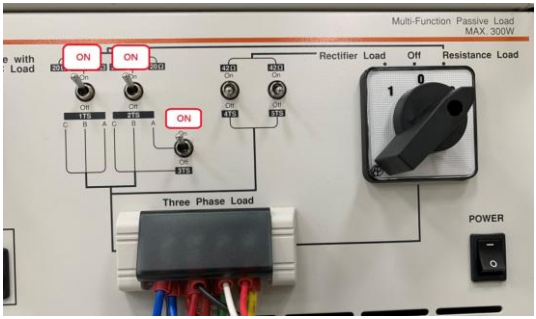


Figure 5.19 Oscilloscope measured waveform when full load

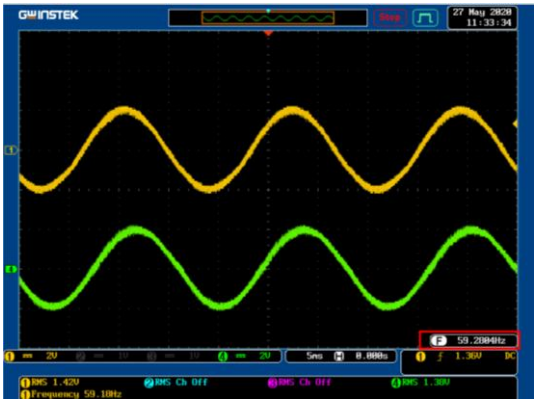
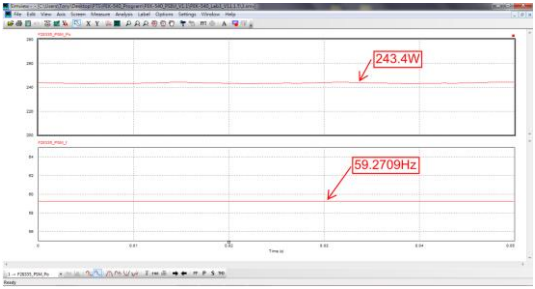


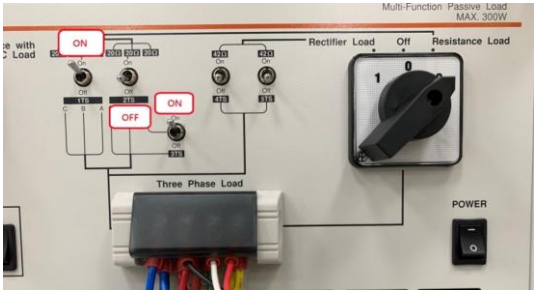
Figure 5.20 DSP oscilloscope measured waveform when full load



2. Q Control

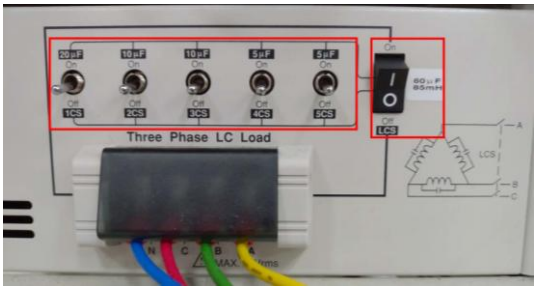
The figure 5.21 shows that 1Ts and 3TS of GPL-500 are set ON, whereas 2TS is set OFF, which indicates half load.

Figure 5.21 GPL-500 half-load setting



As the figure 5.22 shown, the operation steps of GPL-600 is as follows. Power on LCS → Turn on capacitor CS in accord with actual requirement.

Figure 5.22 GPL-600 operation steps



(1) GPL-600 LCS and Capacitor are OFF

As the figure 5.23 and 5.24 shown, when GPL-600 LCS and capacitor are OFF, it is observable that reactive power is 1.775W, whilst VLL voltage is 50.046V.

Figure 5.23 GPL-600LCS and capacitor OFF

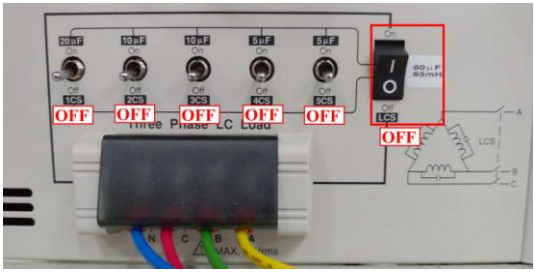
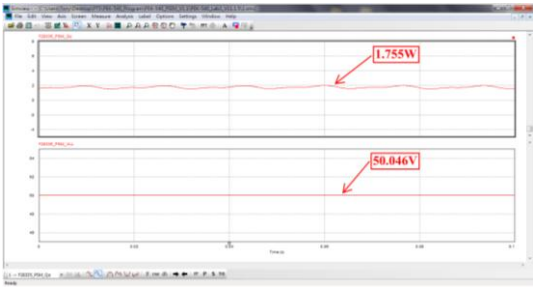


Figure 5.24 DSP oscilloscope waveforms



(2) GPL-600 LCS and Capacitor are ON

As the figure 5.25 and 5.26 shown, when GPL-600 LCS and capacitor are ON, it is observable that reactive power is -122.02W, whilst V_{LL} voltage is 50.665V.

Figure 5.25 GPL-600LCS and capacitor ON

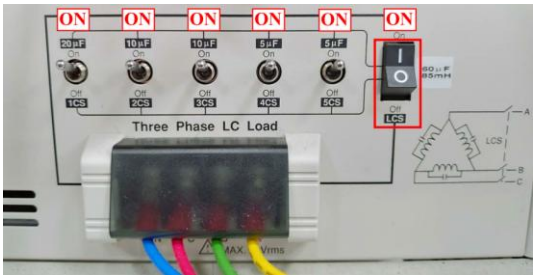


Figure 5.26 DSP oscilloscope waveforms

After experiment, power off PEK-530→PSW160-7.2→PEK-005A→ GPL-500→GPL-600 in order properly.

Under the settings of no-load, half-load and full-load of GPL-500, fill in the table 5.1 with the measured frequency f in order.

Table 5.1 P control frequency measured data

GPL-500	f (frequency)
No load	60.0Hz
Half load	59.6Hz
Full load	59.2Hz

Per differed settings of GPL-500 half-load and GPL-600, fill in the table 5.2 with the reactive power Q and line voltage V_{LL} in order.

Table 5.2 Q control three phase output voltage measured data

GPL-600	Q (reactive power)	V_{LL} (line voltage)
LCS and capacitor OFF	1.755W	50.046V
LCS and capacitor ON	−122.02W	50.665V

The Conclusion

From the experiment, it is known that when active power is raising, via droop control, frequency is decreasing. When, on the other hand, reactive power is decreasing, line voltage V_{LL} is raising.

Experiment 6 – Parallel Operation of Multiple Stand-alone Inverters with Virtual Impedance and Drop Control Method

Circuit Simulation

Inverter Specification	DC Voltage V_{DC} = 100V
	F_s = 18kHz，V_{tri} = 10V_{pp} (PWM)
	C_d = 330uF，L = 1mH，C = 10uF
	K_s = 0.3 (AC current sensing factor)
	K_v = 1/60 (DC voltage sensing factor)
	K_v = 1/40 (DC voltage sensing factor)

The analogue circuit diagram based on the parameters above is as the following figure 6.1 shown:
PSIM File: PEK-530_Sim6_3P_SA_Inv_Parallel_VIDCM(60Hz)_V11.1.5_V1.1

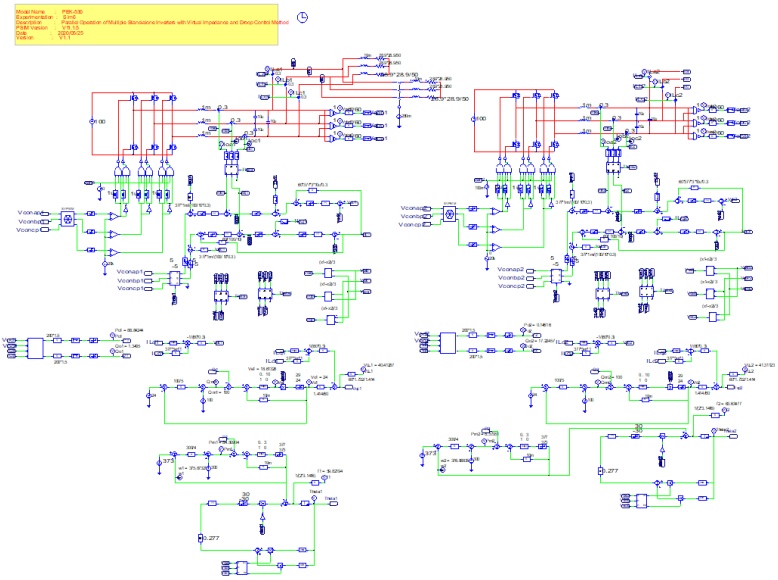


Figure 6.1 Experiment 6 PSIM analogue circuit diagram

The simulating results are shown as the figure 6.2 and 6.3:

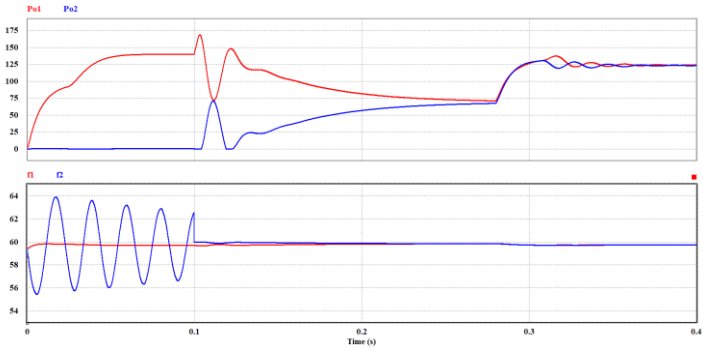


Figure 6.2 Experiment 6 analogue circuit simulation waveforms

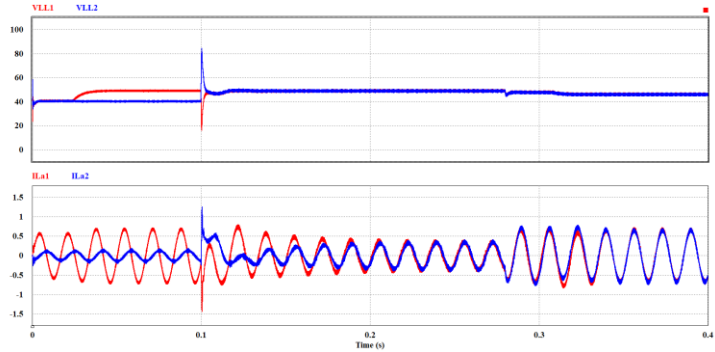


Figure 6.3 Experiment 6 analogue circuit simulation waveforms

The digital circuit diagram based on the analogue circuit is shown as the figure 6.4:

PSIM File: PEK-530_Lab6-1_3P_SA_Inv_Parallel_VIDCM_ Master(60Hz)_V11.1.5_V1.1

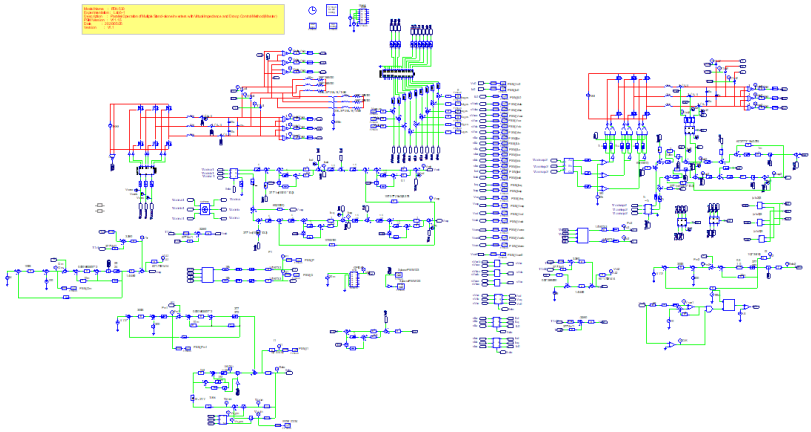


Figure 6.4 Experiment 6 Master PSIM digital circuit diagram

The simulating results are shown as the figure 6.5 and 6.6:

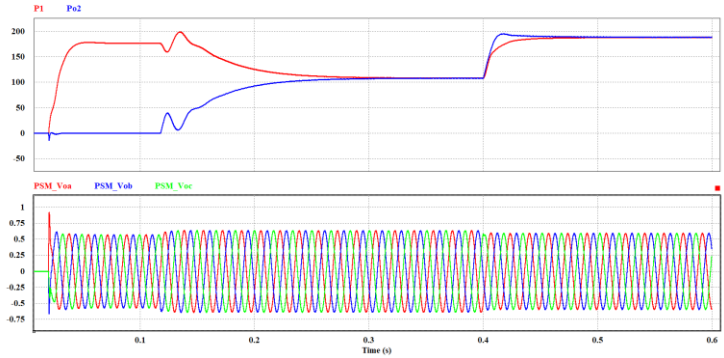


Figure 6.5 Experiment 6 Master digital circuit simulation waveforms

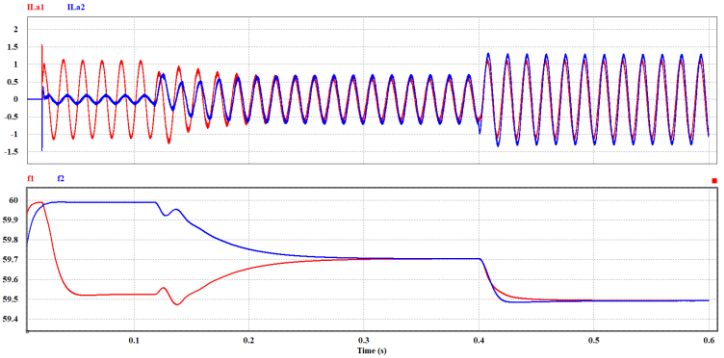


Figure 6.6 Experiment 6 Master digital circuit simulation waveforms

The digital circuit diagram based on the analogue circuit is shown as the figure 6.7:
PSIM File: 530_Lab6-2_3P_SA_Inv_Parallel_ VIDCM_Slave (60Hz)_V11.1.5_V1.15_V1.1

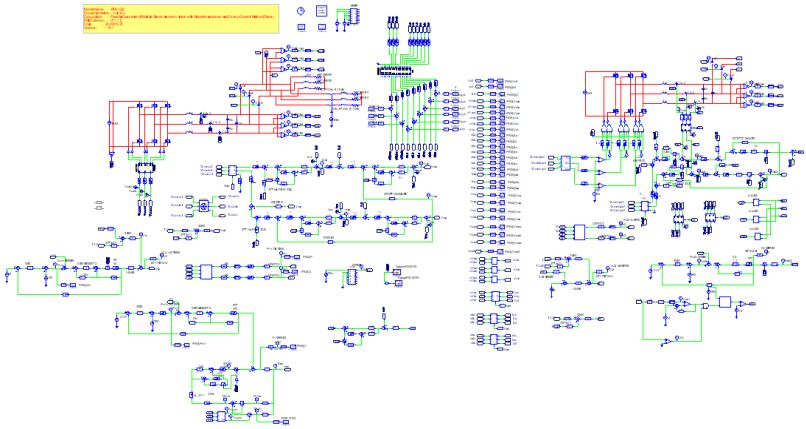


Figure 6.7 Experiment 6 PSIM Slave digital circuit diagram

After confirming the simulating result is identical with Master circuit diagram, the corresponding C Code will be generated automatically via “Generate Code” of “Simulate”.

Experiment Devices

The required devices for experiment are as follows. Refer to user manuals of each device before operation:

- PEK-530 * 1
- PEK-005A * 1
- PEK-006 * 1
- PTS-5000 * 1 (with GDS-2204E, PSW160-7.2 and GPL-500)
- PC * 1

Experiment Procedure

1. The experiment wiring is shown as the figure 6.7. Please follow it to complete wiring.

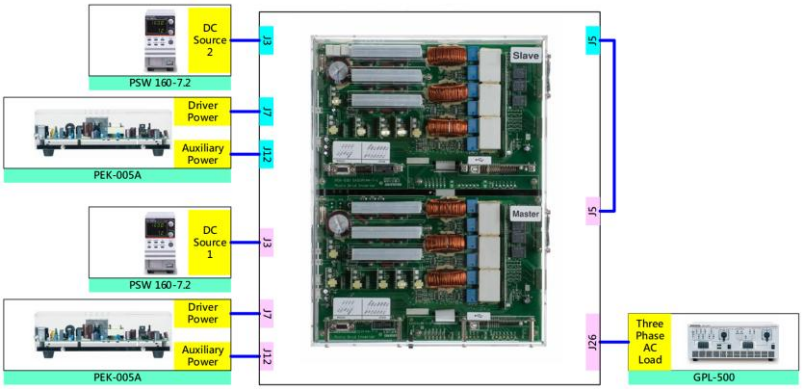


Figure 6.8 Experiment 6 wiring figure

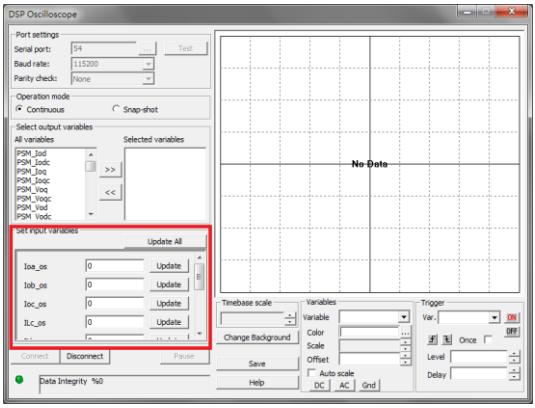
2. After wiring, make sure the PEK-530 switches of Master and Slave are OFF followed by turning the PEK-005A switch ON. The DSP red indicator lights on as the figure 6.9 shown, which means the DSP power is steadily normal.

Figure 6.9 DSP normal status with light on

3. Refer to the appendix B for burning procedure followed by the appendix C for RS232 connection.

4. Parameter Calibration
   As the figure 6.10 shown, PSIM DSP ocsilloscope initial command is 0. If the measured paramter deviates from 0 point, please callibrate the measured parameter back to 0 via adjusting command value.

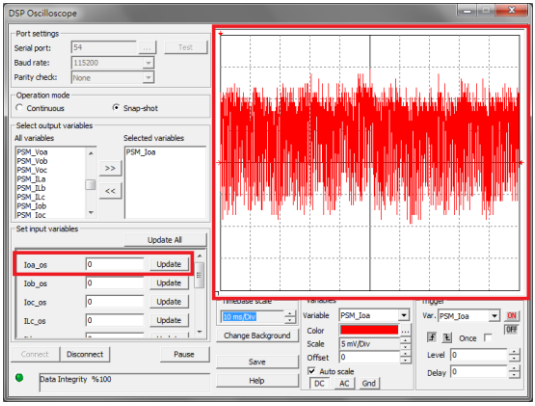
Figure 6.10 The calibration command for measured parameter



- Master Parameter Callibration:

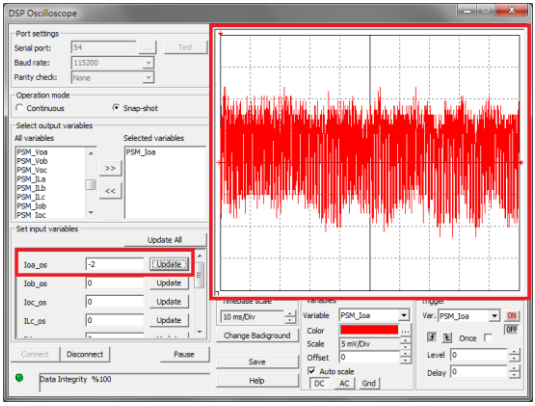
A. As the figure 6.11 shown, the waveform of A phase output current parameter, PSM_Ioa, has deviation from the zero point. Hence, it is required to make waveform approached to zero point via adjustion of initial command parameter, Ioa_os.

Figure 6.11 PSM_Ioa initial measured waveform



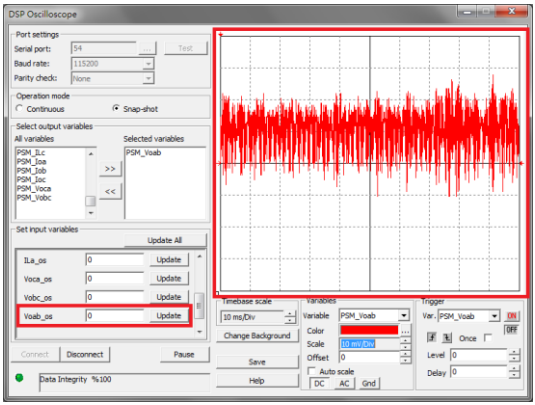
As the figure 6.12 shown, adjust command parameter, Ioa_os, to -2 and it has seen that waveform is in proximity of zero point.

Figure 6.12 PSM_Ioa measured waveform after calibration



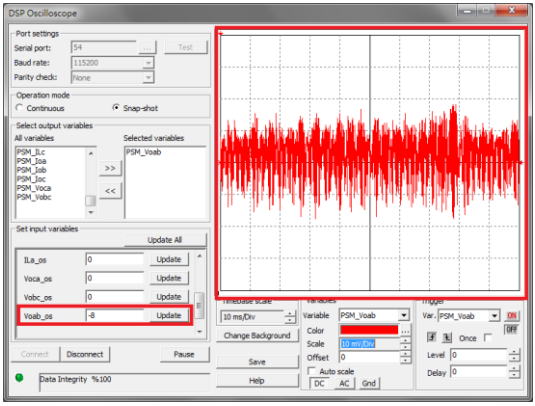
B. As the figure 6.13 shown, the waveform of AB arm line voltage parameter, PSM_ Voab, has deviation from the zero point. Hence, it is required to make waveform approached to zero point via adjustion of initial command parameter, Voab_os.

Figure 6.13 PSM_Voab initial measured waveform



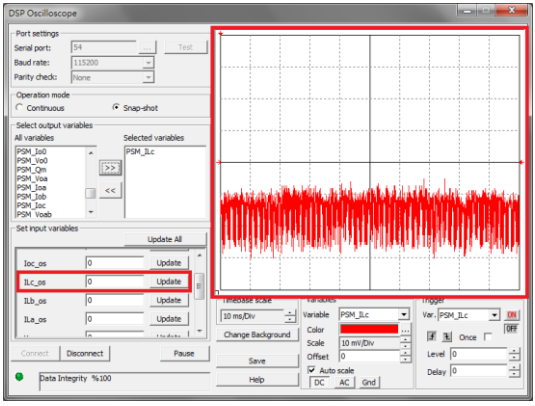
As the figure 6.14 shown, adjust command parameter, Voab_os, to -8 and it has seen that waveform is in proximity of zero point.

Figure 6.14 PSM_Voab measured waveform after calibration



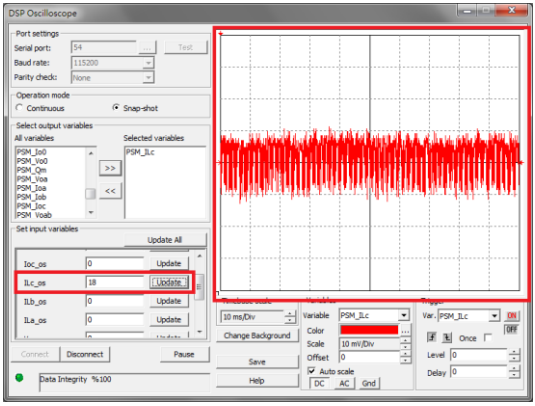
C. As the figure 6.15 shown, the waveform of C phase load current parameter, PSM_ILc, has deviation from the zero point. Hence, it is required to make waveform approached to zero point via adjustion of initial command parameter, ILc_os.

Figure 6.15 ILc initial measured waveform



As the figure 6.16 shown, adjust command parameter, ILc_os, to 18 and it has seen that waveform is in proximity of zero point.

Figure 6.16 ILc measured waveform after calibration



D. The rest parameters of Master including Io-B, Io-C, Vo-BC, Vo-CA, IL-A and IL-B can be calibrated by the above methods.

E. After calibration, the values within the following table 6.1 can be obtained (Calibration values vary per different machine. Also, calibration values of Master and Slave vary)

Table 6.1 Master calibration values of each parameter

Calibration Parameter	Calibration Value
Ioa	-2
Iob	1
Ioc	-3
ILa	3
ILb	3
ILc	18
Voab	-8
Vobc	-8
Voca	-10

F. As the figure 6.17 shown, after calibration, relaunch PSIM file, PEK-530_Lab6-1_3P_SA_Inv_Parallel_VIDCM_Master(60Hz)_V11.1.5_V1.1, followed by filling in the table 6.1 with calibration values for each parameter. Finally, save the file and regenerate C Code.

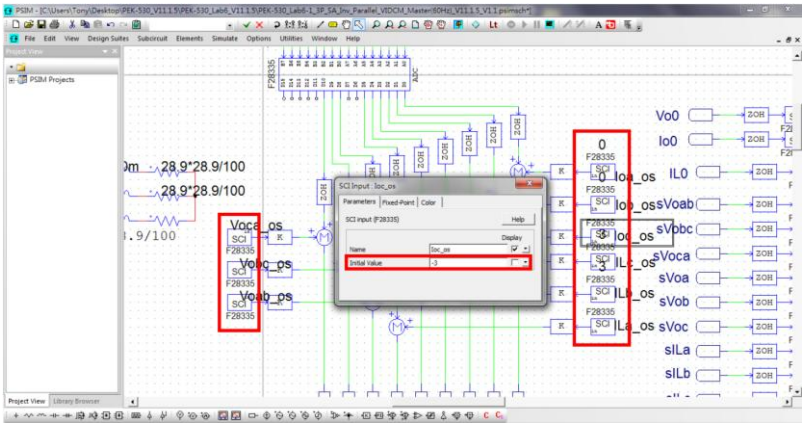
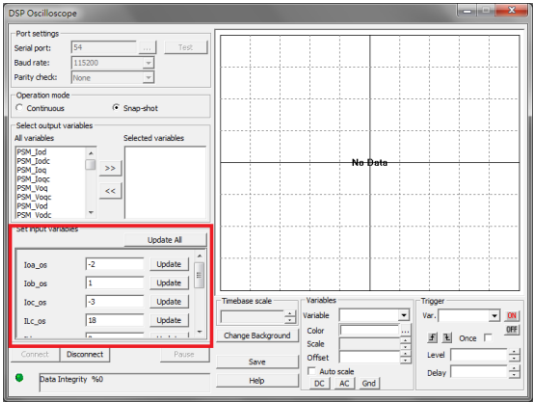


Figure 6.17 Fill in calibration values for each parameter

G. Refer to the appendix B to remove the file PEK-530_Lab6-1 existed in CCS. Again, burn the calibrated C Code generated by PSIM file into DSP as the figure 6.18 shown where each calibration value for each parameter is well written into DSP.

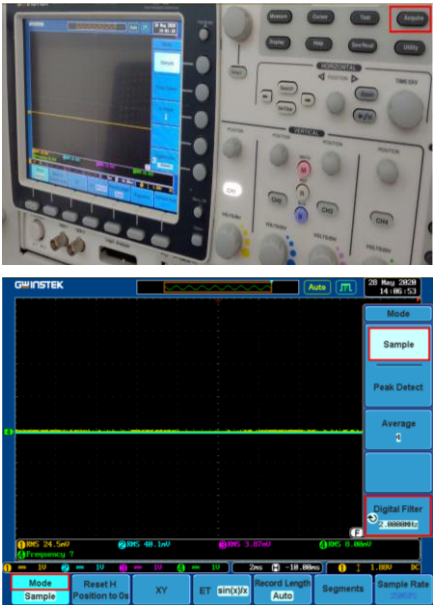
Figure 6.18 Each parameter command value being calibrated



- Slave Parameter Callibration:
  Refer to the previous steps of Master for Slave calibration.

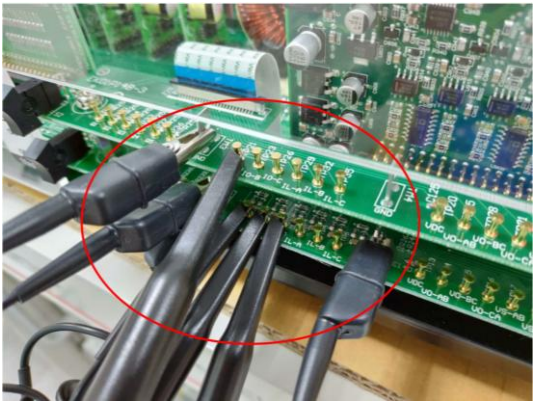
5. The Digital Filter function of oscilloscope is required for this experiment . As the figure 6.19 shown, the setup process is as follows: Acquire→Mode→Sample→Digital Filter. Also, set filter frequency as 2MHz.

Figure 6.18 Setup of Digital Filter of oscilloscope



6. As the figure 6.20 shown, connect the test leads of oscilloscope to Io-A, Io-B and Io-C of Master and Io-A of Slave. Also, connect the GND of test lead to Master GND and Slave GND, respectively.

Figure 6.20 Oscilloscope test leads wiring

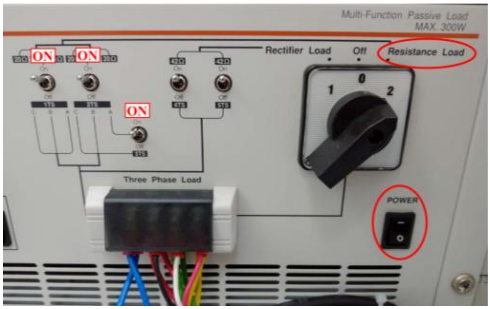


7. Refer to the figure 6.21 for the operation steps of PSW160-7.2. Power on PSW160-7.2→Click on Set key followed by adjusting voltage to 100V via voltage knob and adjusting current to 4A via current knob.

Figure 6.21
The settings of PSW

8. As the figure 6.22 shown, follow the steps below for GPL-500 operation. Power on GPL-500 → Rotate the Three Phase Lord knob to 2 (Resistance Load) → Set 1TS, 2TS and 3TS as OFF, which indicates full-load mode.

Figure 6.22
The full-load setting of GPL-500



After setup, power on 2 sets of PSW power output, respectively, followed by turning on the switches of PEK-530 Master and Slave

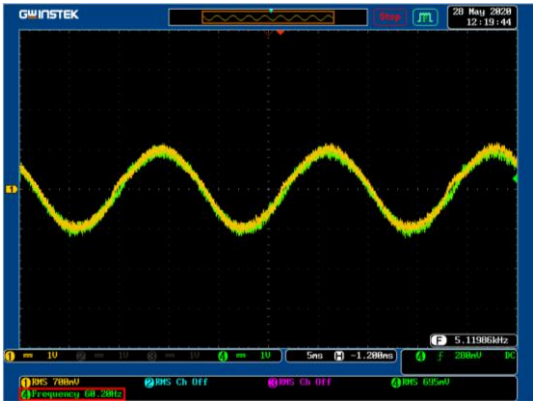
The purpose of experiment

This experiment is the inverter parallel system, which observes the average current effect from 2 sets of inverters via virtual impedance and drop control method.

The experiment result

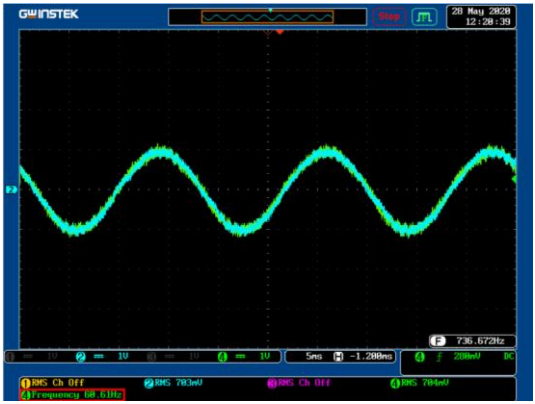
The figure 6.23 shows that RMS value of Master Io-A is 0.7A (1.468A in actual value), and RMS value of Slave Io-A is 0.695A (1.458A in actual value).

Figure 6.23 Master and Slave Io-A measured waveform



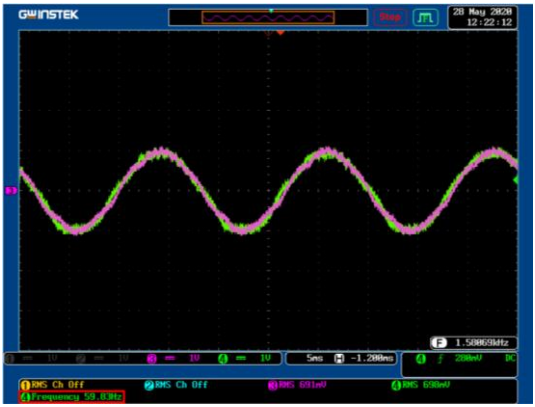
The figure 6.24 shows that RMS value of Master Io-B is 0.703A (1.474A in actual value), and RMS value of Slave Io-B is 0.704A (1.477A in actual value).

Figure 6.24 Master and Slave Io-B measured waveform



The figure 6.25 shows that RMS value of Master Io-C is 0.691A (1.449A in actual value), and RMS value of Slave Io-C is 0.698A (1.464A in actual value).

Figure 6.25 Master and Slave Io-C measured waveform



From the measured waveforms of figures 6.23 through 6.25, the average current effect for 2 sets of inverters is met after command value calibration.

The figure 6.26 shows that RMS value of Master Io-A is 0.708A (1.485A in actual value), RMS value of Io-B is 0.705A (1.479A in actual value), and RMS value of Io-C is 0.694A (1.456A in actual value).

The figure 6.27 shows that RMS value of Slave Io-A is 0.689A (1.445A in actual value), RMS value of Io-B is 0.695A (1.458A in

actual value), and RMS value of Io-C is 0.703A (1.474A in actual value).

Figure 6.26 Master three phase current measured waveform

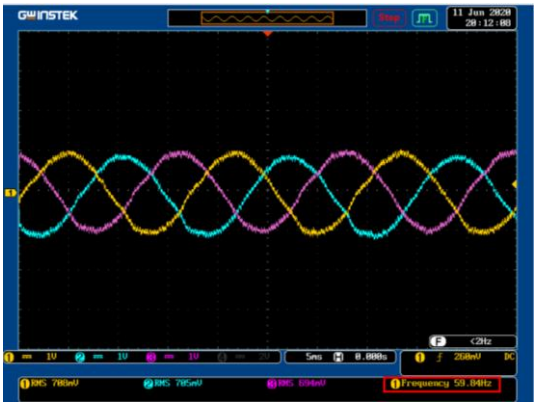
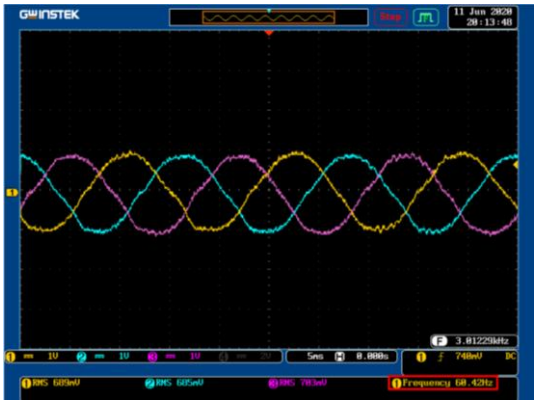


Figure 6.27 Slave three phase current measured waveform



From the balanced waveform shown in the figure 6.26 and 6.27, it is clear that three phase current of 2 sets of inverters are maintained balanced, respectively, after command value calibration.

After experiment, power off switches of Master and Slave of PEK-530→PSW160-7.2→PEK-005A→ GPL-500 in order properly.

Full in the table 6.2 with measured current Io-A, Io-B and Io-C of Master and Slave. Also, refer to the table 0.1 for sensing ratio followed by filling in the actual values.

Table 6.2 Output current measured data in parallel mode

PEK-530	Vo-A(Vrms) (Measured value)	Vo-A(Vrms) (Actual value)	Vo-B(Vrms) (Measured value)	Vo-B(Vrms) (Actual value)
Master	0.708A	1.485A	0.705A	1.479A
Slave	0.689A	1.445A	0.695A	1.458A

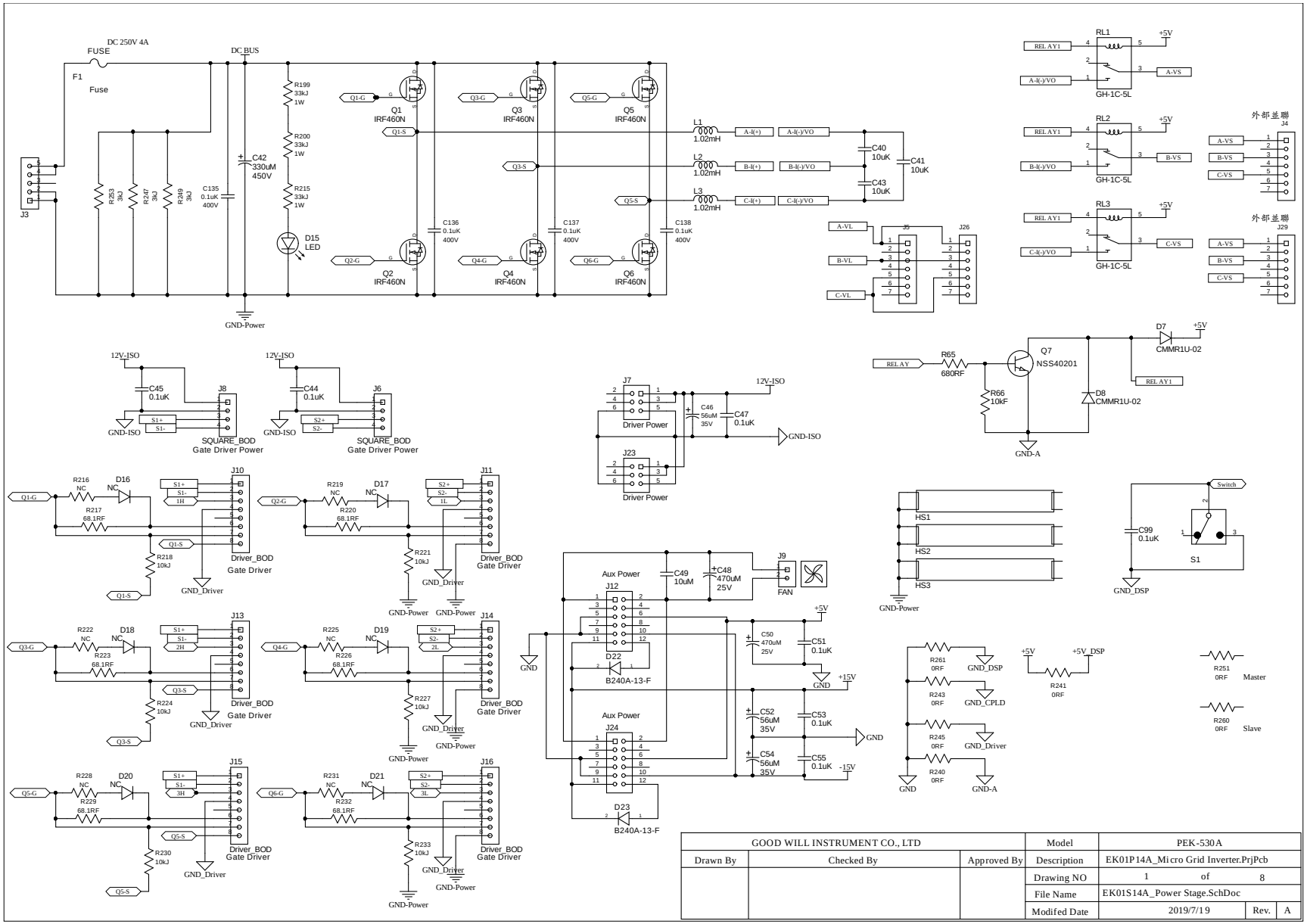
PEK-530	Vo-C(Vrms) (Measured value)	Vo-C(Vrms) (Actual value)
Master	0.694A	1.456A
Slave	0.703A	1.474A

The Conclusion

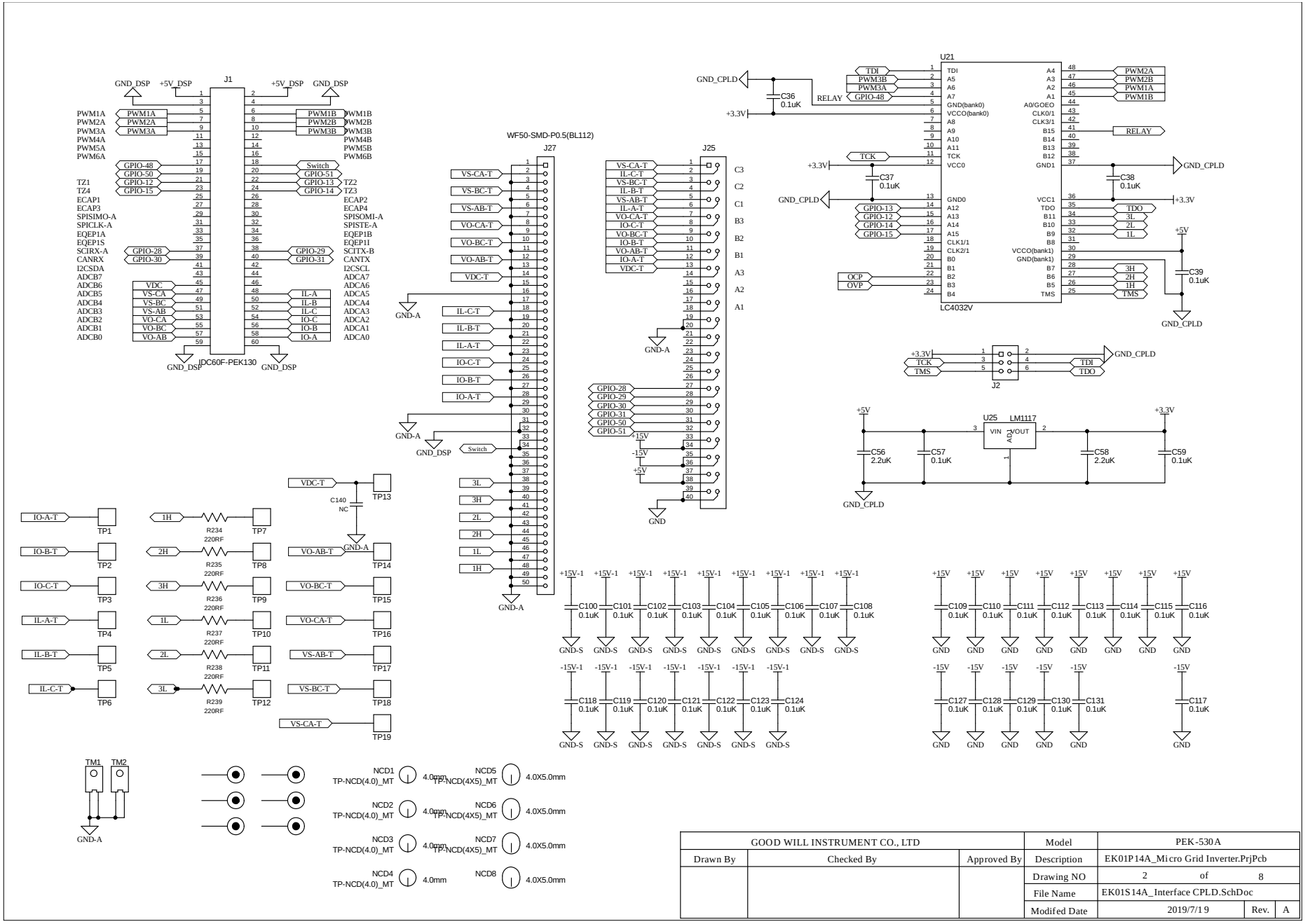
This experiment refers to 2 sets of three phase inverters in parallel. Via virtual impedance and drop control, it has seen that the current of 2 sets of inverters and the individual three phase current are maintained average current.

Appendix A – PEK-530 Circuit Diagram

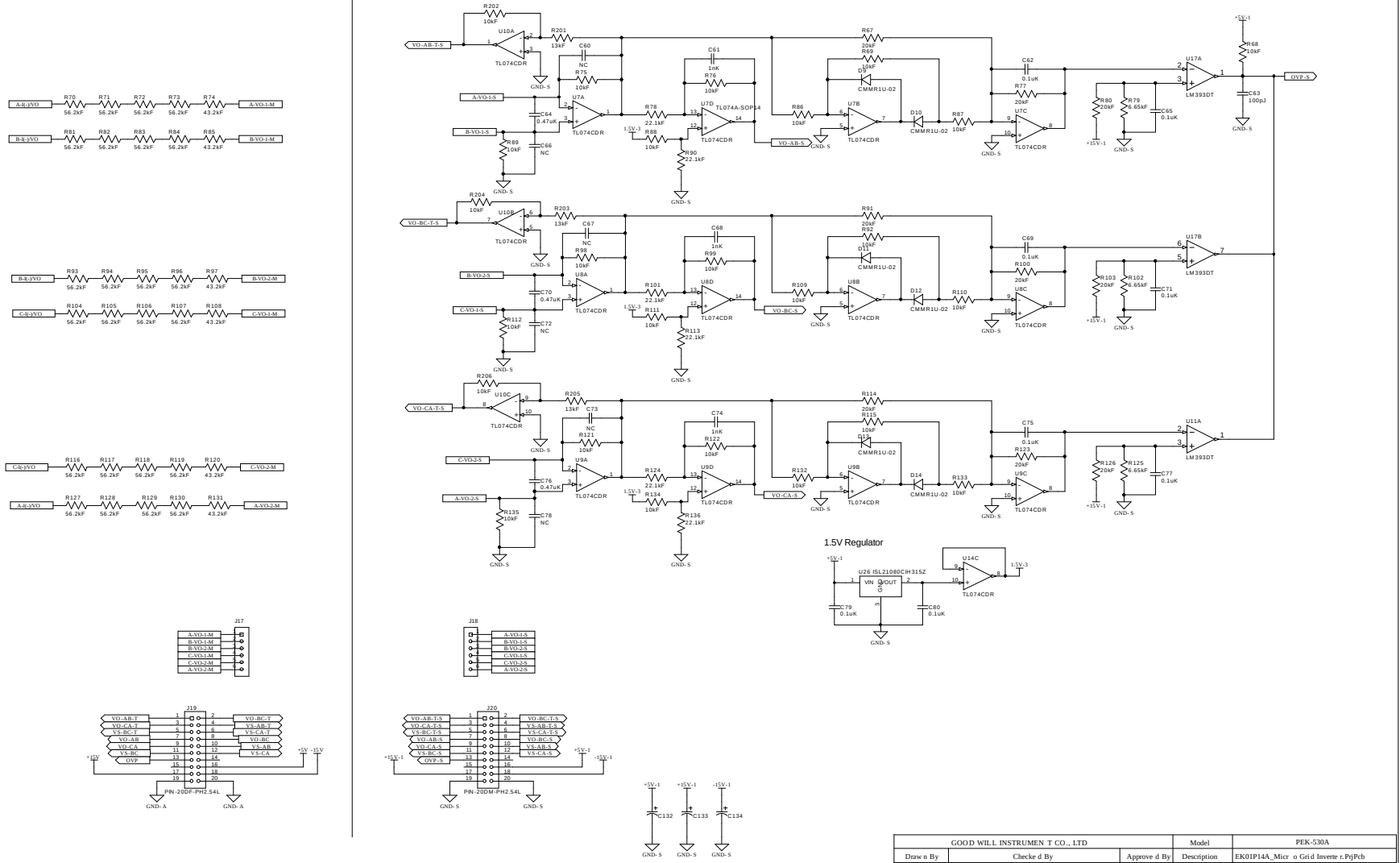
Micro Grid Inverter



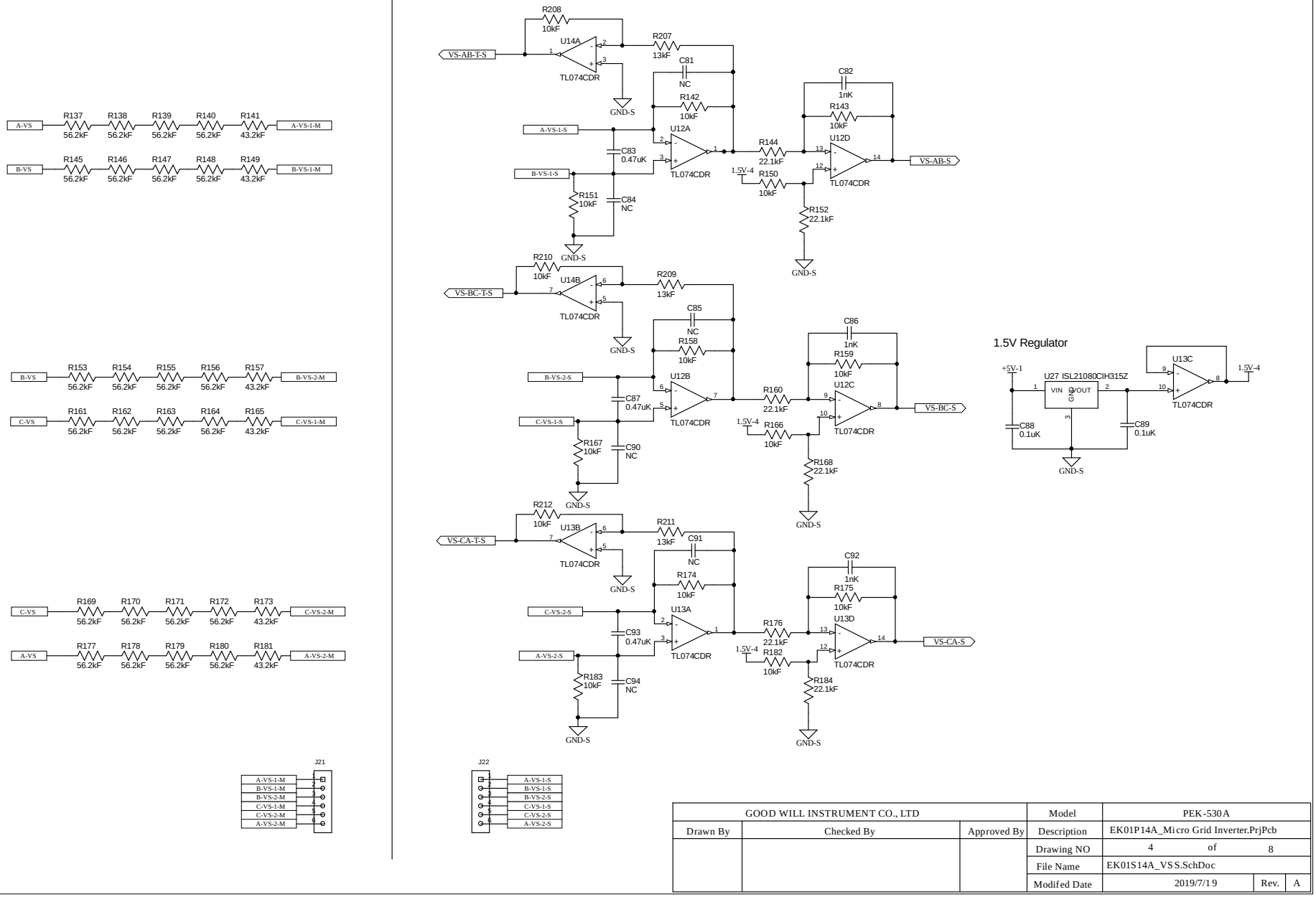
GOOD WILL INSTRUMENT CO., LTD			Model	PEK-530A	
Drawn By	Checked By	Approved By	Description	EK01P14A_Micro Grid Inverter.PrjPcb	
			Drawing NO	1 of 8	
			File Name	EK01S14A_Power Stage.SchDoc	
			Modifed Date	2019/7/19	Rev. A



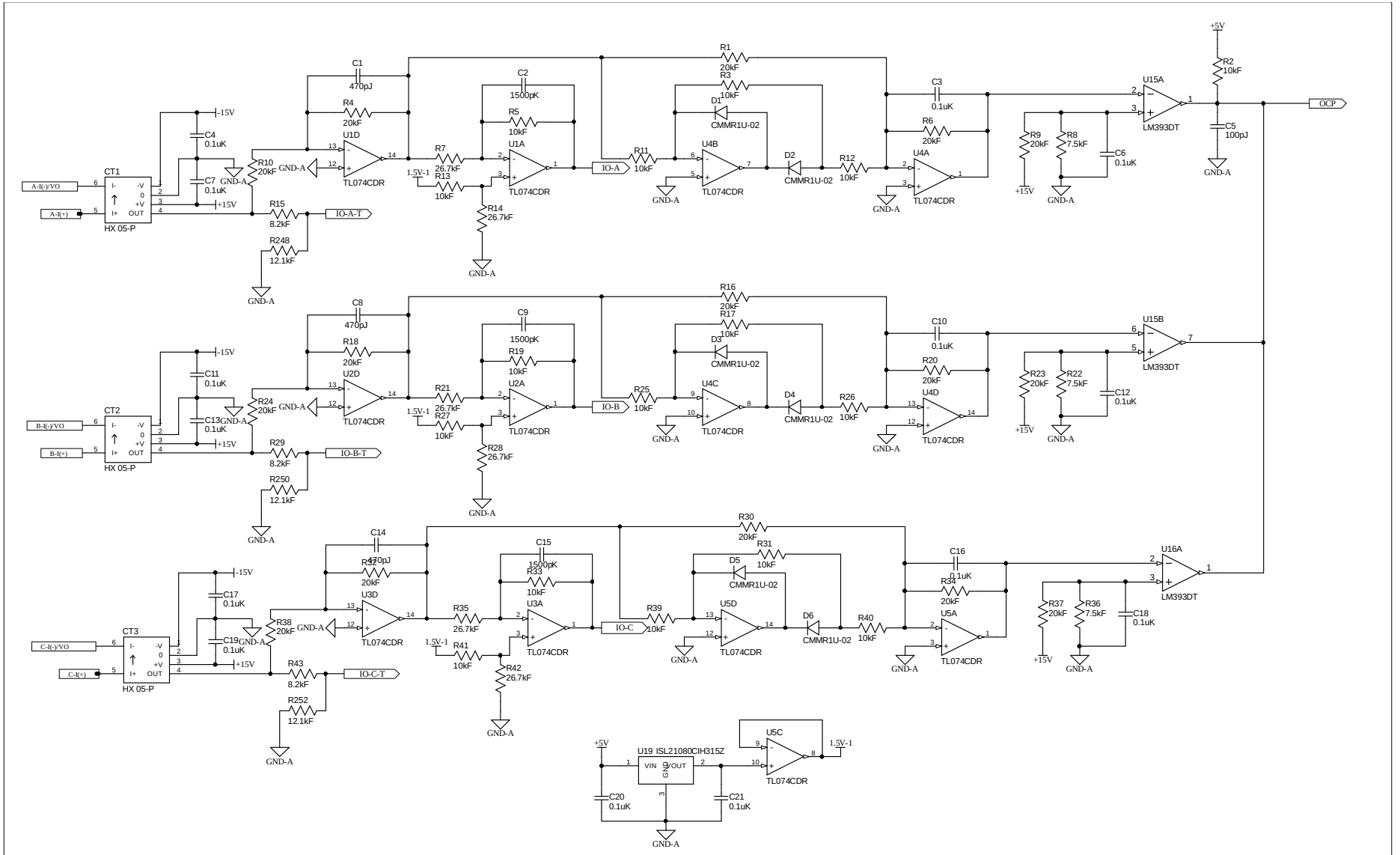
GOOD WILL INSTRUMENT CO., LTD			Model	PEK-530A	
Drawn By	Checked By	Approved By	Description	EK01P14A_Micro Grid Inverter.PrjPcb	
			Drawing NO	2 of 8	
			File Name	EK01S14A_Interface CPLD.SchDoc	
			Modifed Date	2019/7/19	Rev. A



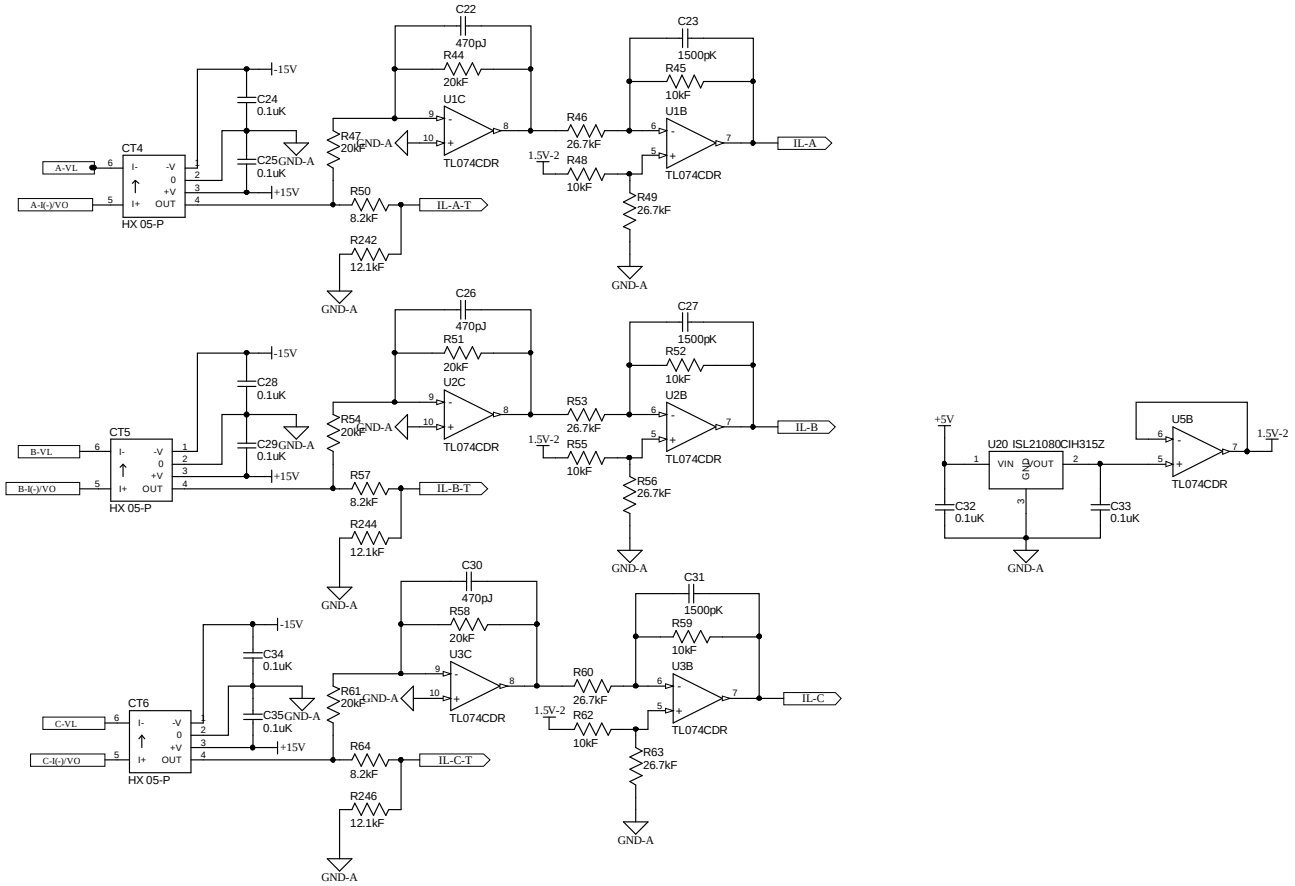
GOOD WILL INSTRUMEN T CO., LTD			Model	PEK-530A
Drawn By	Checke d By	Approve d By	Description	EK01P14A_Micr o Grid Inverte r.PrjPcb
			Drawin g NO	3 of 8
			File Name	EK01S14A_VOS-OV P.SchDoc
			Modife d Date	2019/7/19 Rev. A



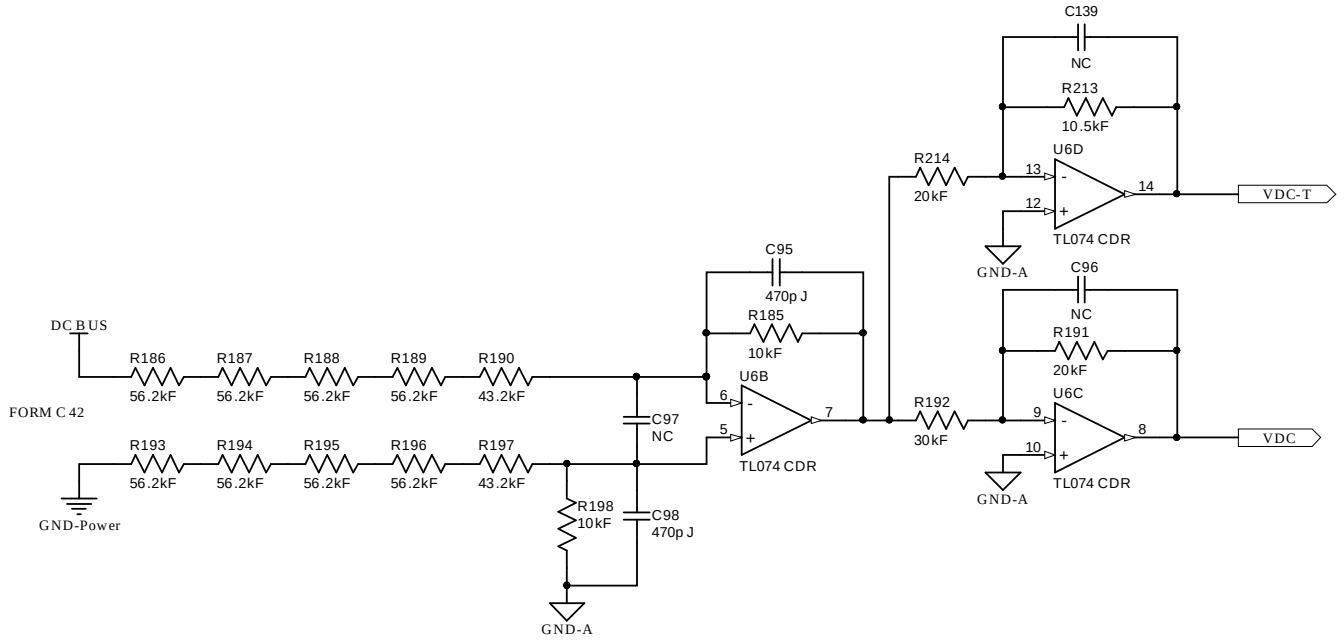
GOOD WILL INSTRUMENT CO., LTD			Model	PEK-530A
Drawn By	Checked By	Approved By	Description	EK01P14A_Micro Grid Inverter.PrjPcb
			Drawing NO	4 of 8
			File Name	EK01S14A_VSS.SchDoc
			Modifed Date	2019/7/19 Rev. A



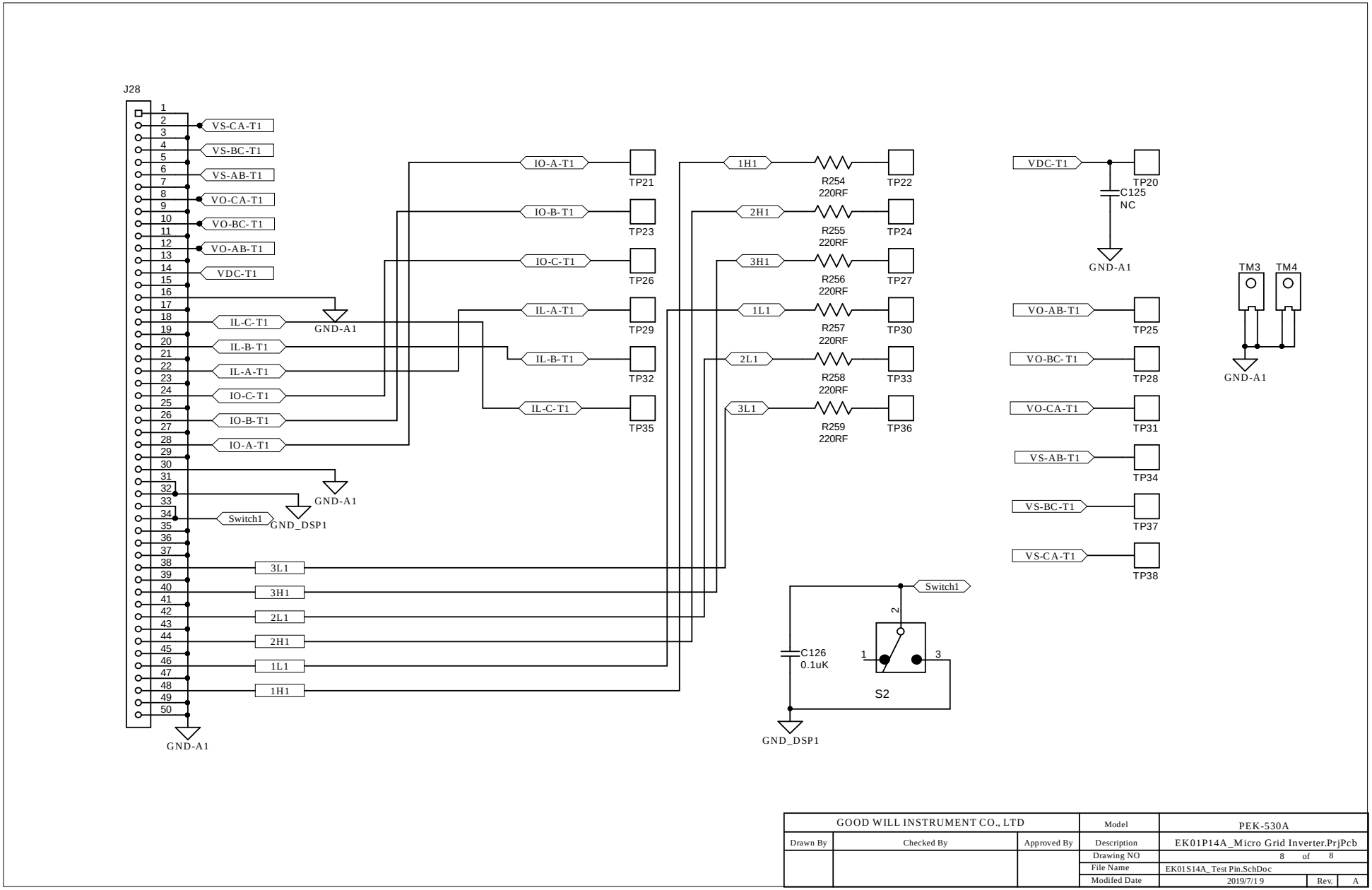
GOOD WILL INSTRUMENT CO., LTD			Model	PEK-530A
Drawn By	Checked By	Approved By	Description	EK01P14A_Micro Grid Inverter.PrjPcb
			Drawing NO	5 of 8
			File Name	EK01S14A_IOS-OCP.SchDoc
			Modifed Date	2019/7/19 Rev. A



GOOD WILL INSTRUMENT CO., LTD			Model	PEK-530A	
Drawn By	Checked By	Approved By	Description	EK01P14A_Micro Grid Inverter.PrjPcb	
			Drawing NO	6 of 8	
			File Name	EK01S14A_ILS.SchDoc	
			Modifed Date	2019/7/19	Rev. A

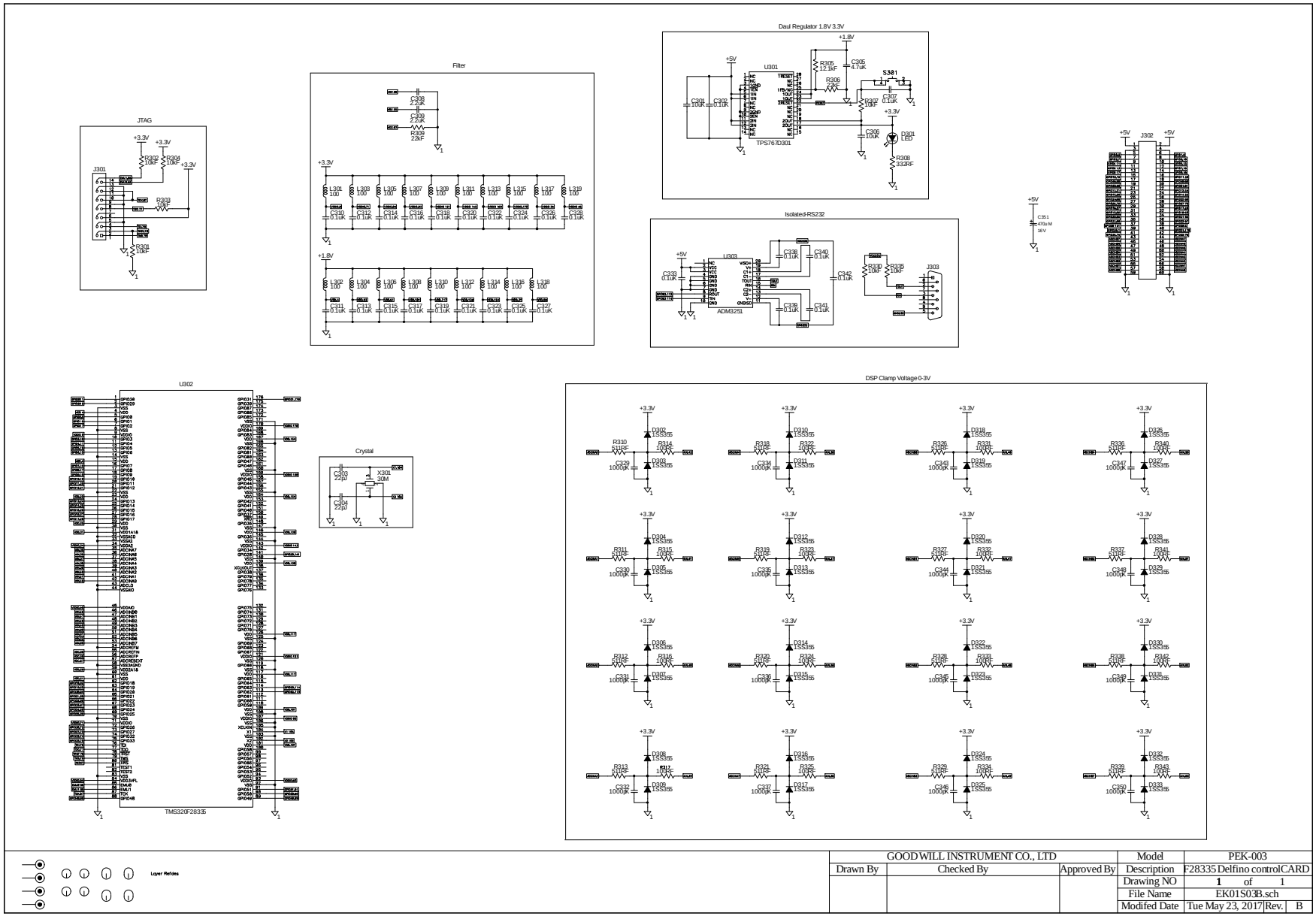


GOOD WILL INSTRUMENT CO., LTD			Model	PEK-530A		
Drawn By	Checked By	Approved By	Description	EK01P14A_Micro Grid Inverter.PrjPcb		
			Drawing NO	7 of 8		
			File Name	EK01S14A_VIS.SchDoc		
			Modifed Date	2019/7/19	Rev.	A

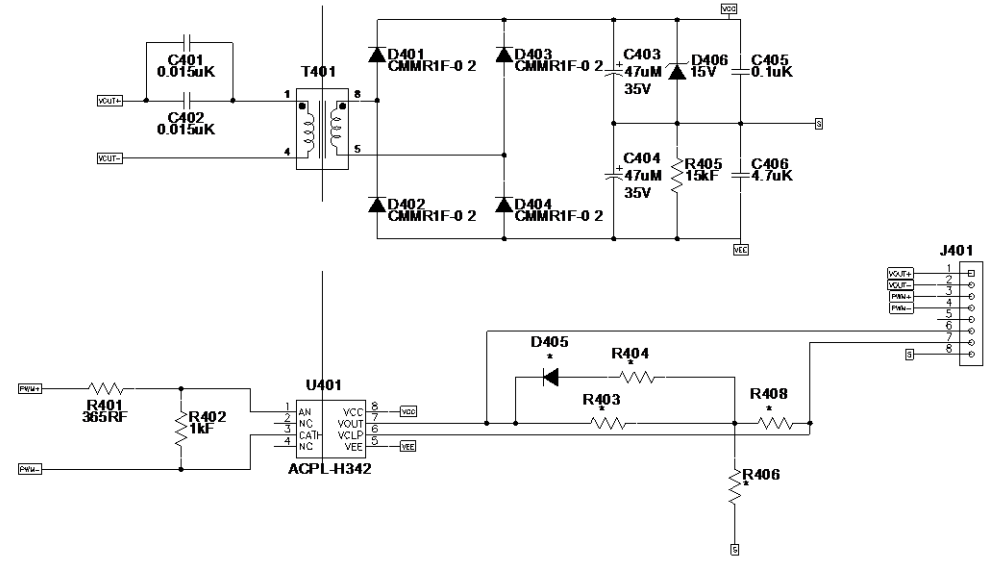


GOOD WILL INSTRUMENT CO., LTD			Model	PEK-530A
Drawn By	Checked By	Approved By	Description	EK01P14A_Micro Grid Inverter.PrjPcb
			Drawing NO	8 of 8
			File Name	EK01S14A_Test Pin.SchDoc
			Modifed Date	2019/7/19 Rev. A

F28335 Delfino control CARD



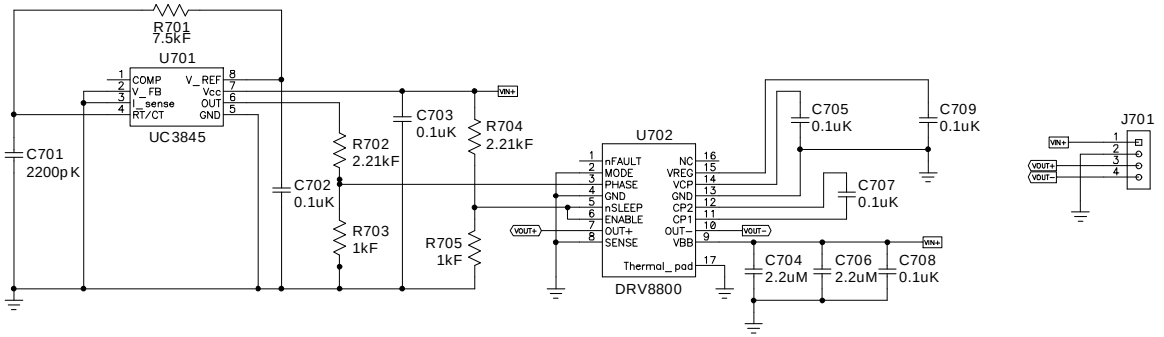
Gate Driver



Layer Refdes

GOOD WILL INSTRUMENT CO., LTD			Model	PEK-004		
Drawn By	Checked By	Approved By	Description	Gate Driver		
			Drawing NO	1 of 1		
			File Name	EK01S04B.sch		
			Modifed Date	Fri May 19, 2017	Rev.	B

Gate Driver Power



Layer Refdes

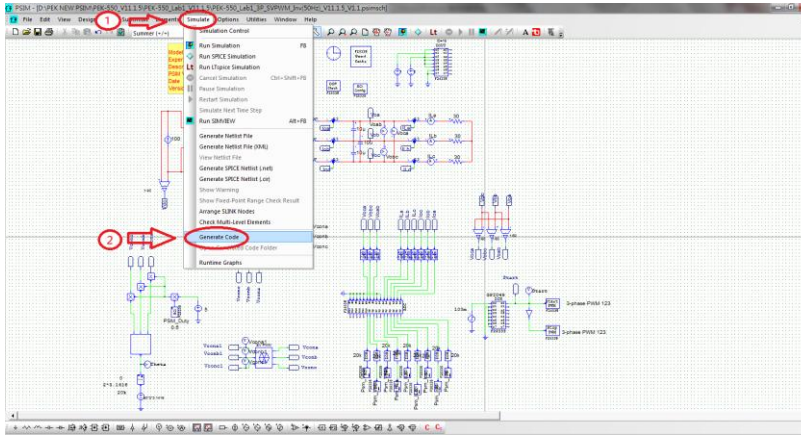
GOOD WILL INSTRUMENT CO., LTD			Model	PEK-100	
Drawn By	Checked By	Approved By	Description	Gate Driver Power	
			Drawing NO	1 of 1	
			File Name	EK01S07A.sch	
			Modifed Date	Mon Mar 09, 2015	Rev. A

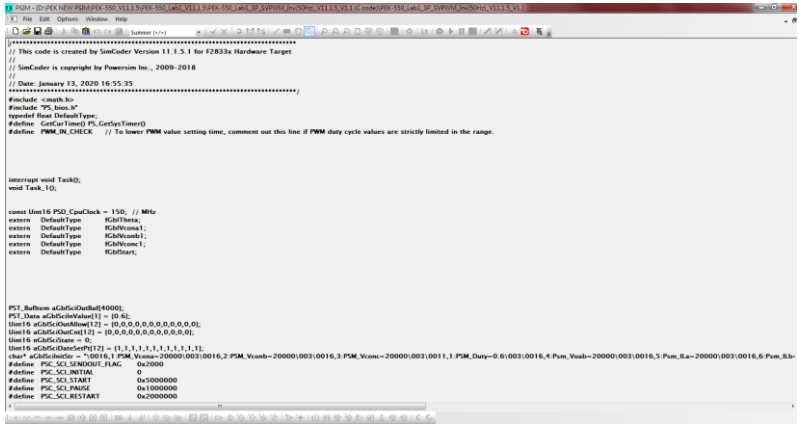
Appendix B – C Code Burning Procedure

This appendix takes "PEK-550_Lab1_3P_SVPWM _Inv(50Hz)_V11.1.5_V1.1" as an example for the instruction. See the detailed steps below.

Operating steps

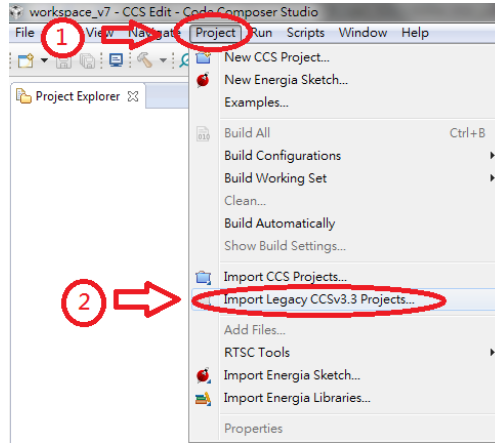
1. Open the digital circuit file "PEK-550_Lab1_3P_SVPWM_Inv(50Hz)_V11.1.5_V1.1 " within the PSIM program followed by clicking "Generate Code" from "Simulate" tab. The PSIM will generate C Code automatically as shown below.



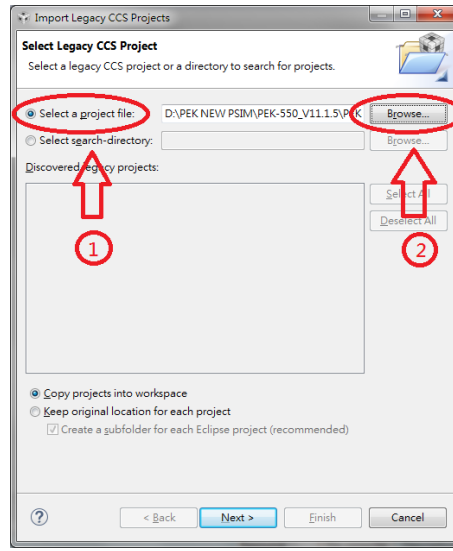


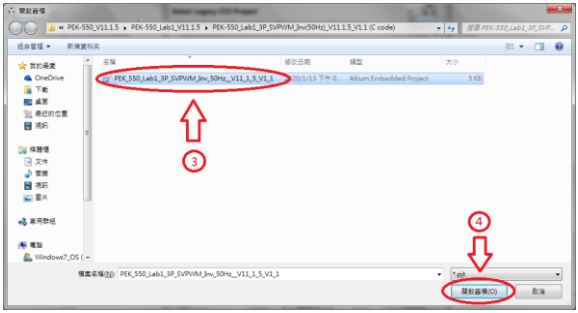
2. A folder of identical name with the PSIM circuit file in which the required files for burning and C Code are well saved will be generated in the location of PSIM circuit file by system.

3. Open CCS and select “Project” tab followed by clicking ”Import Legacy CCSv3.3 Projects” as the figure below.

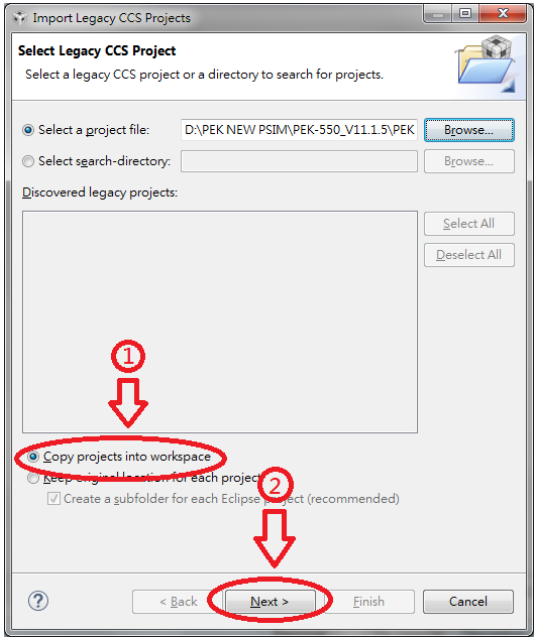


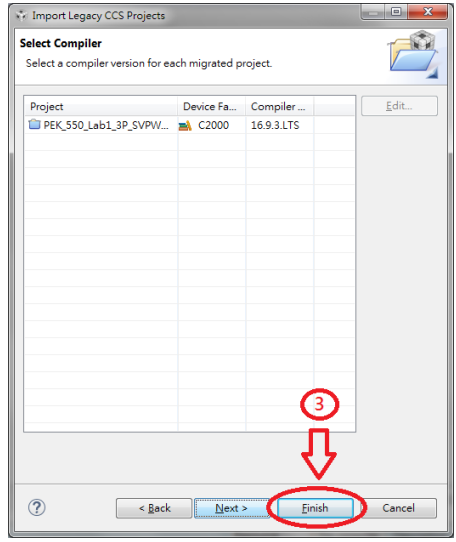
4. Go to "Select a project file" and click "Browser" followed by searching the folder where C Code is located and selecting the file with name extension ".pjt" as the following figure shown.

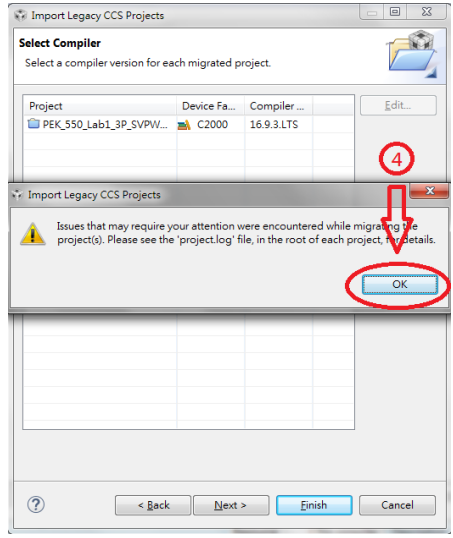




5. Select " Copy projects into workspace " followed by clicking "Next" and then "Finish" to import C Code into CCS program. See the figure below.




Import Legacy CCS Projects
Select Compiler
Select a compiler version for each migrated project.
Project
Device Fa...
Compiler ...
PEK_550_Lab1_3P_SVPW...
C2000
16.9.3.LTS
Edit...
3
< Back
Next >
Finish
Cancel


Import Legacy CCS Projects
Select Compiler
Select a compiler version for each migrated project.
Project
Device Fa...
Compiler ...
PEK_550_Lab1_3P_SVPW...
C2000
16.9.3.LTS
Edit...
4
Import Legacy CCS Projects
Issues that may require your attention were encountered while migrating the project(s). Please see the 'project.log' file, in the root of each project, for details.
OK
< Back
Next >
Finish
Cancel

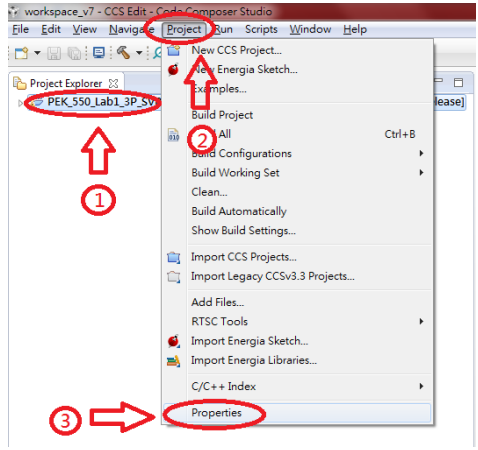
6. Select C Code file and choose “Properties” from “Project” tab. The setting steps are as follows.

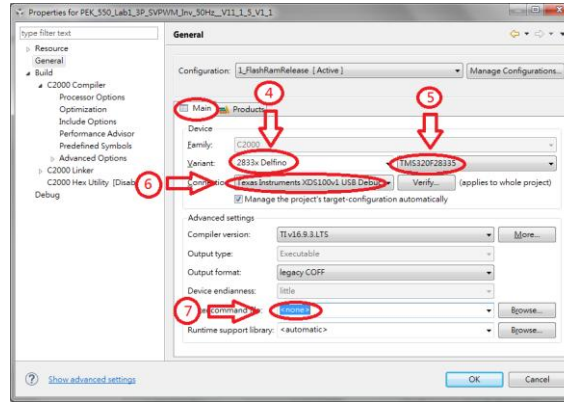
   1) Select “TMS320F28335” of “2833X Delfino” from Variant under Main tab.

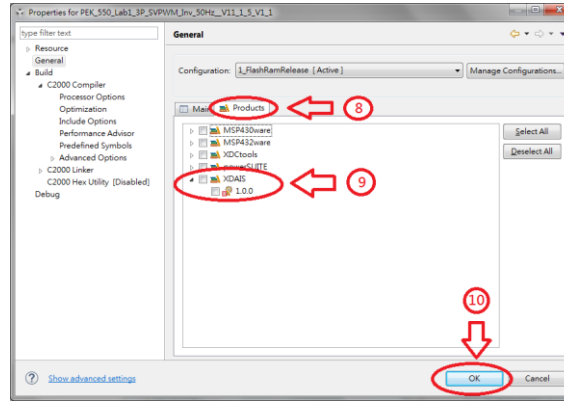
   2) Select “Texas Instruments XDS100v1 USB Debug Probe” from Connection under Main tab.

   3) Select “none” from Linker command file under Main tab.

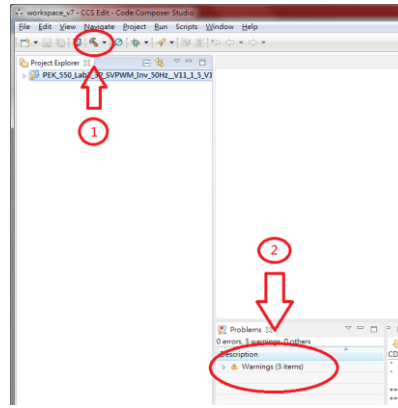
   4) Deselect “XDAIS” under Project tab. (Ignore this step if your CCS version doesn’t provide this option.



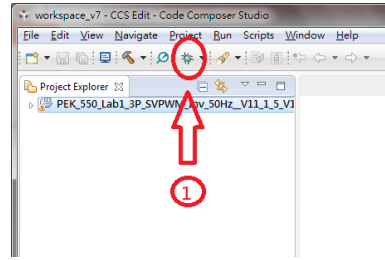




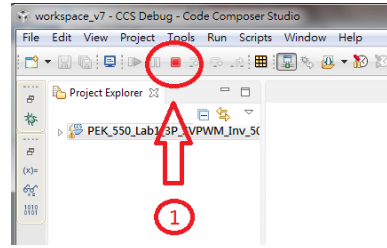
7. After the setting, click “Build” for compilation. If no errors occur after compiling, the program is eligible for burning. Simply ignore the warnings, which have no impact on burning process.



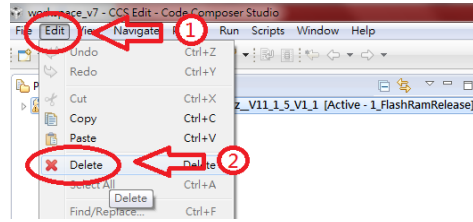
8. Connect PEK-006 to PC and PEK module respectively followed by clicking “Debug” to proceed to burning process.

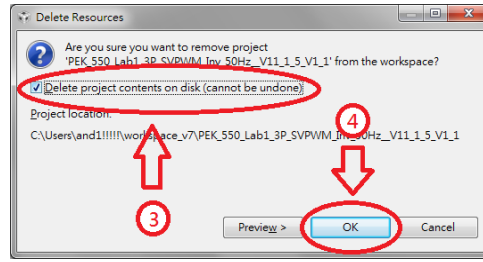


9. After the burning process, click "Terminate" and remove "PEK-006"to finish the entire procedure.



10. If it needs to delete file, select C Code file followed by selecting "Delete" under "Edit" tab and checking "Delete project contents on disk". Finally, click "OK" to complete the action.



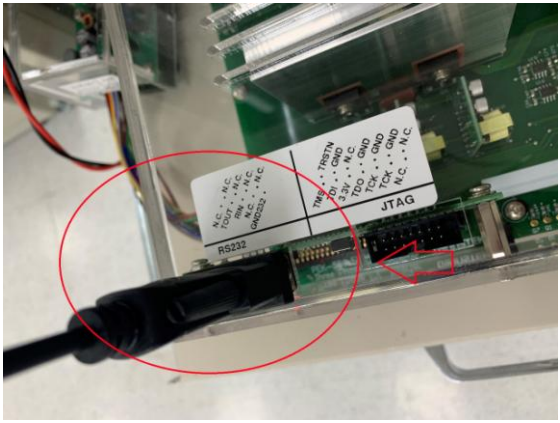


Appendix C – RS232 Connection

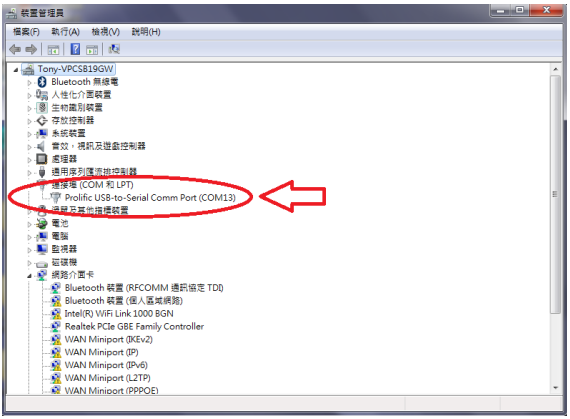
Operating steps

1. Connect PEK-005A to PEK module and make sure DSP is working normally.

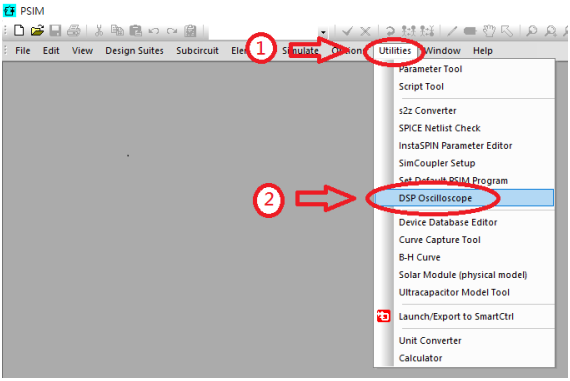
2. Connect one end of RS232 cable to PC, and the other end to the RS232 connector of PEK module.



3. Open Device Manger from PC and identify the COM port number being utilized by RS232 cable.



4. Open PSIM program and select “DSP Oscilloscope” under “Utilities” tab.

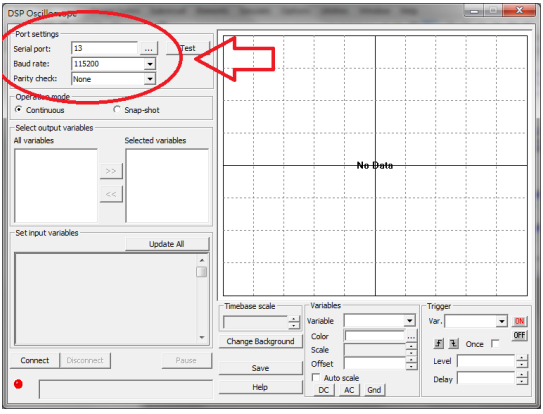


5. The Port settings are as follows.

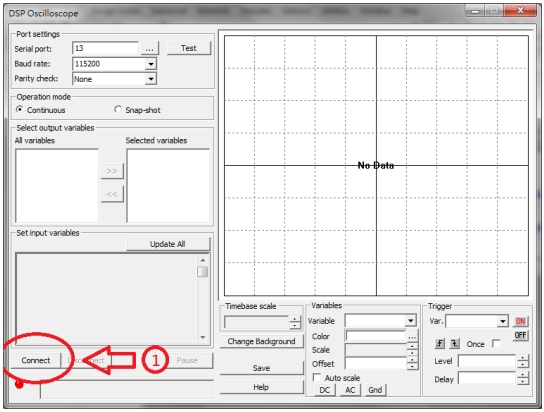
   1) Select the COM port being used by RS232.

   2) Set 115200 for Baud rate.

   3) Set None for Parity check.



6. After the settings, click "Connect" to proceed to RS232 connection.



7. Both the output and input variables schemed within PSIM circuit can be clearly observed when connection is properly established.