Three-Phase PV Inverter Developer's Kit

PEK-550

User Manual

GW INSTEK PART NO. 82EK-11000M01

ISO-9001 CERTIFIED MANUFACTURER

GW INSTEK

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Introduction

As the figure 0.1 shown, PEK-510, the Three Phase PV Inverter Module, is based on both the first-stage structure of Boost Converter and the second-class structure of Three Phase Three Wire Inverter with fully digital control system. The purpose of it, as shown in the figure 0.2, is to provide a learning platform for power converter of specifically digital control, having users, via PSIM software, to understand the principle, analysis as well as design of power converter through simulating process. More than that, it helps convert, via SimCoder tool of PSIM, control circuit into digital control and proceed to simulation with the circuit of DSP, eventually burning the control program, through simulating verification, in the DSP chip. Also, it precisely verifies the accuracy of designed circuit and controller via control and communication of DSP.

Figure 0.1

Experiment module of Three Phase PV Inverter Module

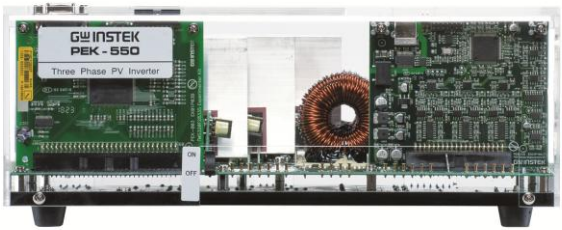
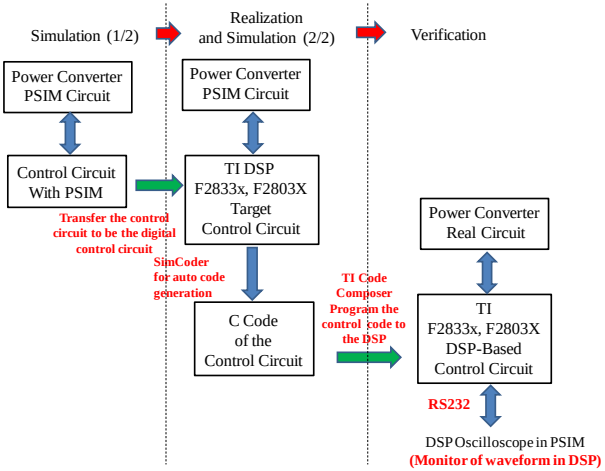


Figure 0.2

The process in details



There are 6 experiments can be fulfilled by PEK-550 as follows:

1. Three Phase SVPWM Inverter
2. Three Phase Boost Stand-alone Inverter
3. Three Phase Grid-connected Inverter
4. PV Boost Converter
5. Three Phase Islanding Protection Inverter
1. Three Phase PV Grid-connected Inverter

In addition to PEK-550, it is required to utilize PEK-005A auxiliary power module as figure 0.3 shown and PEK-006 JTAG burning module as figure 0.4 shown for experiments. Also, PTS-5000 experiment platform as figure 0.5 shown is necessary for completing the experiments.

Figure 0.3

Auxiliary power module

Figure 0.4

JTAG burning module

Figure 0.5

PTS-5000 experiment platform

The DSP I/O pin configuration of PEK-550 is shown as the figure 0.6. Refer to the appendix A for the circuit diagrams of PEK-550, which can be divided into power circuit, sensing circuit, drive circuit and protection circuit. The sensing circuit is further divided into 2 sections; one is for test point measurement, and the other one is for feedback DSP control, both of which have varied attenuation amplifications individually as the following table 0-1 and table 0-2 shown.

Figure 0.6

I/O configuration

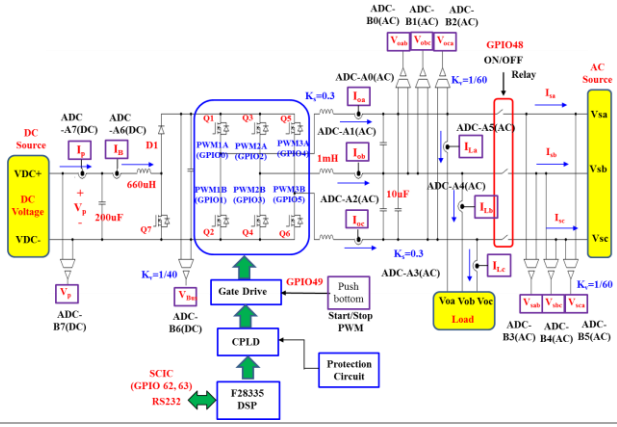


Table 0.1 PEK-550 test point measurement ratio

	Sensing item	Sensing ratio
1	Boost Converter input voltage (Vin)	0.0196
2	DC link voltage (VBUS)	0.0196
3	Boost Converter input current (Iin)	0.4
4	Boost Converter inductor current (IB)	0.4
5	Inverter A phase output current (IO-A)	0.4768
6	Inverter B phase output current (IO-B)	0.4768
7	Inverter C phase output current (IO-C)	0.4768
8	Inverter A phase load current (IL-A)	0.4768
9	Inverter B phase load current (IL-B)	0.4768
10	Inverter C phase load current (IL-C)	0.4768
11	Inverter output AB arm line voltage (VO-AB)	0.0287
12	Inverter output BC arm line voltage (VO-BC)	0.0287

13	Inverter output CA arm line voltage (VO-CA)	0.0287
14	Grid-connected AB arm line voltage (VS-AB)	0.0287
15	Grid-connected BC arm line voltage (VS-BC)	0.0287
16	Grid-connected CA arm line voltage (VS-CA)	0.0287

Table 0.2 PEK-550 DSP feedback ratio

	Sensing item	Sensing ratio
1	Boost Converter input voltage (Vin)	0.0249
2	DC link voltage (VBUS)	0.0249
3	Boost Converter input current (Iin)	0.6
4	Boost Converter inductor current (IB)	0.6
5	Inverter A phase output current (IO-A)	0.2996
6	Inverter B phase output current (IO-B)	0.2996
7	Inverter C phase output current (IO-C)	0.2996
8	Inverter A phase load current (IL-A)	0.2996
9	Inverter B phase load current (IL-B)	0.2996
10	Inverter C phase load current (IL-C)	0.2996
11	Inverter output AB arm line voltage (VO-AB)	0.0169
12	Inverter output BC arm line voltage (VO-BC)	0.0169
13	Inverter output CA arm line voltage (VO-CA)	0.0169
14	Grid-connected AB arm line voltage (VS-AB)	0.0169
15	Grid-connected BC arm line voltage (VS-BC)	0.0169
16	Grid-connected CA arm line voltage (VS-CA)	0.0169

The Description on Chapters

See the chapter arrangements as follows

Brief	Briefly describes the experimental method, experimental items and circuit setup. It also explains the contents of each chapter.
Experiment 1 Three Phase SVPWM Inverter	To get to know the main circuit of three phase inverter, and learn three-phase SPWM, SVPWM as well as three phase axis conversion. To realize the DSP digital control circuit planning and learn the method of digital control programming via PEK-550 module. To well get familiar with the experiment devices and software manipulation.
Experiment 2 Interleaved Boost Converter	To get to know the way for modeling of three phase inverter, and learn the design of both voltage loop and current loop controllers, further proceeding to the code programming via SimCoder, after well mapping out the hardware.
Experiment 3 Bi-directional DC-DC Converter	To get to know the fundamental with structure of three phase grid-connected inverter, and learn not only the design method of phase-lock loop of three phase grid-connected inverter, but the design of both voltage loop and current loop controllers as well, further proceeding to the code programming via SimCoder, after well mapping out the three phase grid connected inverter.
Experiment 4 Three phase Four Wire Boost Stand-alone Inverter	To get to know the characteristics of PV module and diversified MPPT method, and learn the code programming of Perturb and Observe method, further verifying the experiment result via boost converter of PEK-550.

Experiment 5 Three phase Four Wire PV Grid-connected Inverter	To get to know the purpose and way to test verification of PV islanding protection, further proceeding to the code programming via SimCoder, after well mapping out the hardware.
Experiment 6 Three phase Four Wire Battery Energy Storage System	To get to know the fundamental with structure of three phase PV grid-connected inverter, and synthesize boost converter with three-phase inverter to form the experiment of three phase PV grid-connected inverter, further proceeding to the code programming via SimCoder, after well planning.

Experiment 1 – Three Phase SVPWM Inverter

Preview

1. Understand main circuit of three phase inverter
2. Learn three phase SPWM
3. Learn SVPWM
4. Learn three phase axis conversion
5. Get familiar with experiment devices and software manipulation

Experiment Contents and Purpose

1. Output voltage fluctuation under varied load
2. Duty adjustment and observation under open circuit

Principle and Design

Three Phase SPWM

SPWM (Sinusoidal Pulse Width Modulation) theory is to compare three phase sine wave voltage command generated by controller with triangle wave. Through comparator, the generated pulse width modulated signal drives inverter, which will then output the voltage waveform close to sine wave with equal amplitude but with unequal width. Based on scale and frequency of sine wave voltage and triangle wave, the following two indexes can be defined. The first one is Modulation Index as follows:

$$m_a = \frac{\hat{V}_{control}}{\hat{V}_{tri}} \quad (1.1)$$

From the equation above, Vcontrol indicates scale of three phase sine wave voltage peak value, whereas Vtri stands for scale of triangle wave peak value.

The second one is Frequency Modulation Ratio with the definition below:

$$m_f = \frac{f_s}{f_l} \quad (1.2)$$

From the equation above, fs indicates triangle wave frequency, whilst fl stands for sine wave voltage frequency.

Figure 1.1 Three phase inverter circuit

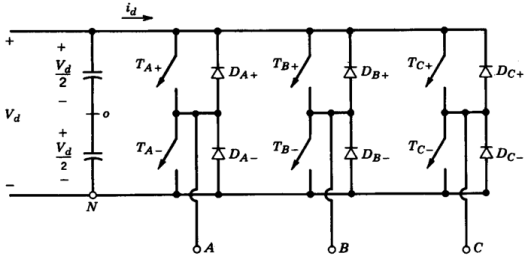
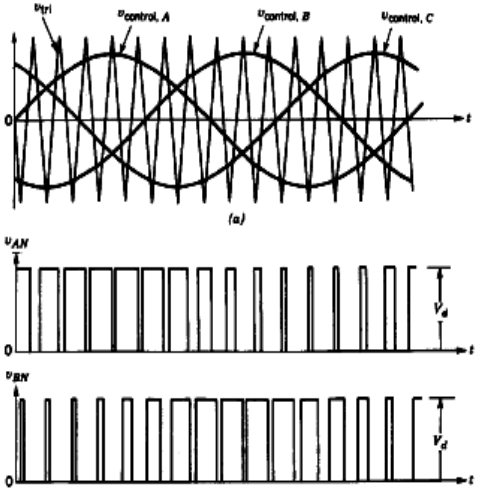
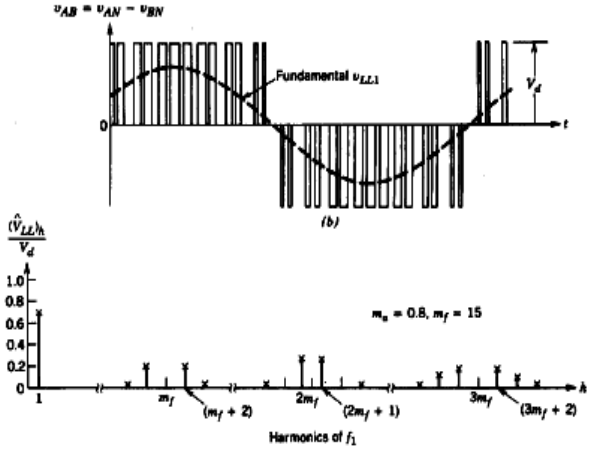


Figure 1.2 SPWM





Take A phase from the figure 1.1 for example, the basic waveform peak value of voltage VAN can be expressed as follows:

$$(\hat{V}_{AN})_1 = m_a \frac{V_d}{2} \tag{1.3}$$

The basic waveform line to line voltage sacle (RMS) is as follows:

$$\begin{aligned} \frac{V_{LL1}}{(\text{line}-\text{line, rms})} &= \frac{\sqrt{3}}{\sqrt{2}}(\hat{V}_{AN})_1 \\ &= \frac{\sqrt{3}}{2\sqrt{2}} m_a V_d \\ &\cong 0.612 m_a V_d \quad (\text{ma} \le 1.0) \end{aligned} \tag{1.4}$$

When ma is less than or equal to 1,the so-called linear modulation area in which peak value of input sine wave voltage command is less than that of triangle wave, the input voltage scale will be in propotion to line to line voltage scale of inverter output voltage basic waveform.

Three Phase Space Vector PWM (SVPWM)

Space vector pulse width modulation utilizes the concept of voltage space vector, generating the rolling voltage vector space via the switch state of 6 power components from inverter. Refer to the figure 1.3 for three phase inverter in which each phase has 2 swtich

components that are placed in upper arm (S1, S3, S5) and lower arm (S2、S4、S6) individually. Under the control mode of space vector pulse width modulation, the conduction state of switch component from each phase of inverter is complementary, which means that if upper arm is in conduction state, the lower arm is in stop state and vice versa. In terms of control, generally, a delayed time, also known as dead time, is added prior to switch conduction in case of power component damage because power components of upper arm and lower arm are in conduction mode simultaneously. We define each arm switch conduction state of a, b and c phase, respectively. When a is equal to 1, upper arm switch is in conduction, and the lower arm switch is in stop state. When a is equal to 0, upper arm switch is in stop state, and the lower arm switch is in conduction. Therefore, output states of three phase inverter are of 8 types, and the output result (DC link voltage = VDC for example) of line to line voltage along with phase voltage generated by each state is listed within the table 1.1.

Figure 1.3

Classic three phase inverter structure

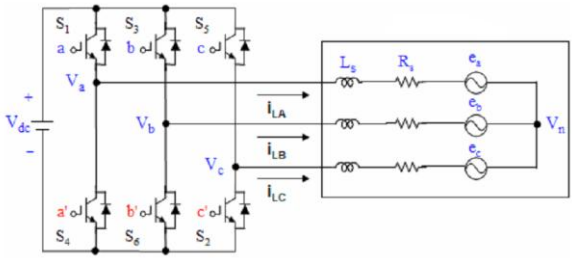


Table 1.1

Swtich states of three phase inverter

Voltage Vectors	Switching Vectors			Line to neutral voltage			Line to line voltage		
	a	b	c	V_{an}	V_{bn}	V_{cn}	V_{ab}	V_{bc}	V_{ca}
V_0	0	0	0	0	0	0	0	0	0
V_1	1	0	0	2/3	-1/3	-1/3	1	0	-1
V_2	1	1	0	1/3	1/3	-2/3	0	1	-1
V_3	0	1	0	-1/3	2/3	-1/3	-1	1	0
V_4	0	1	1	-2/3	1/3	1/3	-1	0	1
V_5	0	0	1	-1/3	-1/3	2/3	0	-1	1
V_6	1	0	1	1/3	-2/3	1/3	1	-1	0
V_7	1	1	1	0	0	0	0	0	0

From the table 1.1 we can realize the relation between line voltage and phase voltage output by three phase inverter. The table 1.2, which further shows the math relation below, is achieved via the coordinate axis conversion to αβ platform.

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (1.5)$$

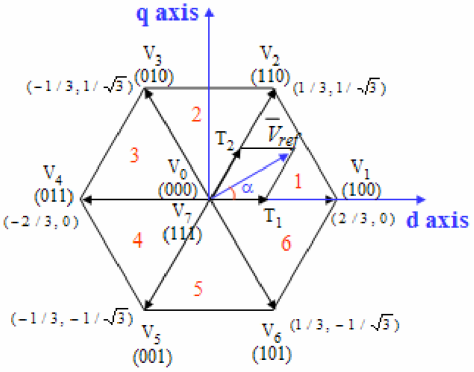
Table 1.2

Switch state

	V_α	V_β
$\vec{V}_0$	0	0
$\vec{V}_1$	$-\frac{V_{DC}}{3}$	$-\frac{V_{DC}}{3}$
$\vec{V}_2$	$-\frac{V_{DC}}{3}$	$\frac{V_{DC}}{3}$
$\vec{V}_3$	$-\frac{2V_{DC}}{3}$	0
$\vec{V}_4$	$\frac{2V_{DC}}{3}$	0
$\vec{V}_5$	$\frac{V_{DC}}{3}$	$-\frac{V_{DC}}{\sqrt{3}}$
$\vec{V}_6$	$\frac{V_{DC}}{3}$	$\frac{V_{DC}}{\sqrt{3}}$
$\vec{V}_7$	0	0

The 8 different voltage vectors, which are the so-called basic voltage vectors, are obtained via the above 8 switch states. Among the 8 voltage vectors, 6 are effective voltage vectors ($\vec{V}_1$, $\vec{V}_2$, $\vec{V}_3$, $\vec{V}_4$, $\vec{V}_5$, $\vec{V}_6$) and the rest 2 are zero vectors ($\vec{V}_0$ and $\vec{V}_7$). Therefore, we take advantage of the 6 effective voltage vectors to divide voltage space platform into 6 sections. As the figure 1.4 shown where is the reference voltage vector for output.

Figure 1.4
Basic vector space



It is available to take any of 2 vectors from the 6 effective voltage vectors within the figure 1.4 to express the output reference voltage $\vec{V}_{ref}$ of any scale. In addition, the output voltage within the 2 effective voltage components of vector (conduction time) can be obtained via algebra.

Axis Conversion

(1) Static Coordinate Axis Conversion

Convert the three phase abc static coordinate axis to static coordinate axis system, which is the so-called Clarke conversion. Refer to the figure 1.5 in which the following coordinate axis conversion equation (1.6) can be obtained via the relation of 2 coordinate systems.

$$\begin{bmatrix} f_\alpha \\ f_\beta \\ f_o \end{bmatrix} = [T] \begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \quad (1.6)$$

Where:

$f_\alpha \cdot f_\beta \cdot f_o$ are the variables from $\alpha\beta$ axis when voltage and current are pending.

$f_a \cdot f_b \cdot f_c$ are the variables from abc axis when voltage and current are pending.

$$[T]=\frac{2}{3}\begin{bmatrix}1 & -\frac{1}{2} & -\frac{1}{2}\\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2}\\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2}\end{bmatrix}$$ is the coordinate axis matrix

In contrast, convert $\alpha\beta$ coordinate axis to three phase abc coordinate axis system, which is the so-called anti-Clarke conversion. The conversion equation is illustrated below:

$$\begin{bmatrix}f_a\\ f_b\\ f_c\end{bmatrix}=[T]^{-1}\begin{bmatrix}f_\alpha\\ f_\beta\\ f_o\end{bmatrix} \quad (1.7)$$

Where:

$$[T]^{-1}=\begin{bmatrix}1 & 0 & 1\\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1\\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1\end{bmatrix}$$ is the coordinate axis matrix

The above describes the relation between three phase abc coordinate system and $\alpha\beta$ static coordinate system,the undetermined coefficient prior to conversion matrix of which is $\frac{2}{3}$ when non-power rule of constant is adopted. If, however, power rule of constant is adopted, the undetermined coefficient turns out $\sqrt{\frac{2}{3}}$. We employ non-power rule of constant hereby. In addition, in terms of three phase balance system, when static coordinate axis conversion is underway, zero sequence component $f_o=\frac{1}{3}(f_a+f_b+f_c)$ is negligible. The figure 1.6 shows the waveform diagram when PSIM is utilized to simulate abc static coordinate axis conversion to static coordinate axis.

Figure 1.5
Static coordinate axis

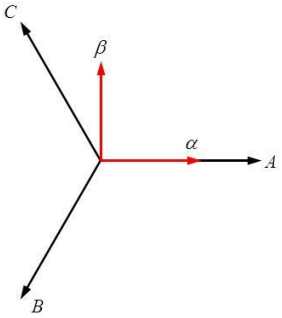
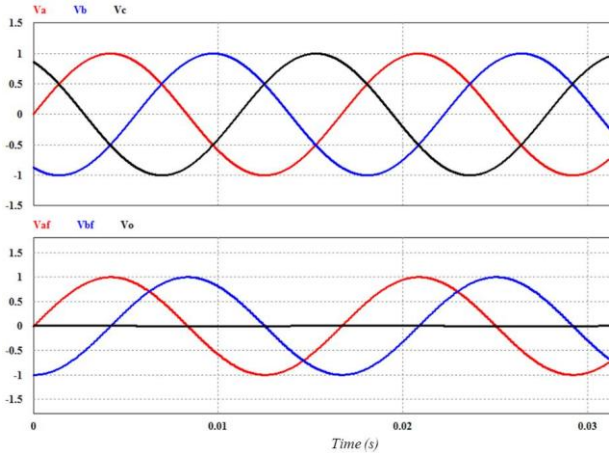


Figure 1.6
Waveform of PSIM simulating static coordinate axis conversion



(1) (2) Synchronous Rotating Coordinate Axis Conversion

From the previous chapter in which we convert abc static coordinate system, via coordinate axis conversion, into $\alpha\beta$ static coordinate axis system. In this chapter we further convert $\alpha\beta$ static coordinate axis into DQ synchronous rotating coordinate axis system, which is called Park conversion. When presuming three phase system is balanced and placing both DQ axis and $\alpha\beta$ axis on the 2-dimentional platform, as the figure 1.7 shown, with neglecting zero axis component, the rotating coordinate is able to rotate in accord with ω_e angle, by which the coordinate conversion formula is obtained as follows:

$$\begin{bmatrix} f_\alpha \\ f_\beta \end{bmatrix} = [Q] \begin{bmatrix} f_d \\ f_q \end{bmatrix} \tag{1.8}$$

Where:

$$[Q]=\begin{bmatrix}\cos(\theta_e) & \sin(\theta_e)\\ -\sin(\theta_e) & \cos(\theta_e)\end{bmatrix}$$

On the contrary, to convert rotating coordinate system DQ axis to $\alpha\beta$ coordinate system is what we called anti-Park conversion, the conversion formula of which is as follows:

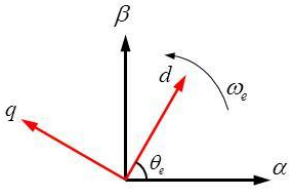
$$\begin{bmatrix}f_d\\ f_q\end{bmatrix}=[Q]^{-1}\begin{bmatrix}f_\alpha\\ f_\beta\end{bmatrix} \quad (1.9)$$

Where:

$$[Q]^{-1}=\begin{bmatrix}\cos(\theta_e) & -\sin(\theta_e)\\ \sin(\theta_e) & \cos(\theta_e)\end{bmatrix}$$

θ_e is the included angle, which is expressed as $\theta_e=\int_0^t \omega_e dt+\theta_e(0)$.

Figure 1.7 Synchronous rotating coordinate axis



(2) (3) Arbitrary Rotating Coordinate Axis Conversion

From the previous two sections, it is understandable that both static coordinate axis conversion and synchronous rotating axis conversion can be projected to DQ coordinate axis via abc coordinate system. As the figure 1.8 shown where coordinate conversion formula is obtained as follows:

$$\begin{bmatrix}f_d\\ f_q\\ f_o\end{bmatrix}=[R]\begin{bmatrix}f_a\\ f_b\\ f_c\end{bmatrix} \quad (1.10)$$

Where:

$$[R]=\frac{2}{3}\begin{bmatrix}\cos(\theta_e) & \cos(\theta_e-\frac{2\pi}{3}) & \cos(\theta_e+\frac{2\pi}{3})\\ -\sin(\theta_e) & -\sin(\theta_e-\frac{2\pi}{3}) & -\sin(\theta_e+\frac{2\pi}{3})\\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2}\end{bmatrix}$$

By contrast, conver rotating coordinate system DQ axis to $\alpha\beta$ coordinate system, which is the so-called anti-Park conversion, the conversion formula of which is shown below:

$$\begin{bmatrix}f_a\\ f_b\\ f_c\end{bmatrix}=[R]\begin{bmatrix}f_d\\ f_q\\ f_o\end{bmatrix} \quad (1.11)$$

Where:

$$[R]^{-1}=\begin{bmatrix}\cos(\theta_e) & -\sin(\theta_e) & 1\\ \cos(\theta_e-\frac{2\pi}{3}) & -\sin(\theta_e-\frac{2\pi}{3}) & 1\\ \cos(\theta_e+\frac{2\pi}{3}) & -\sin(\theta_e+\frac{2\pi}{3}) & 1\end{bmatrix}$$

When assuming it is a three phase balanced syste, the zero phase component $f_o=\frac{1}{3}(f_a+f_b+f_c)$ can be simply neglected.

Figure 1.8 Arbitrary rotating coordinate axis

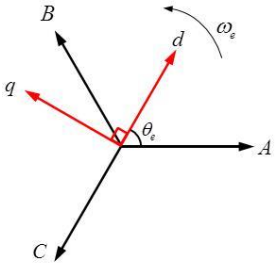
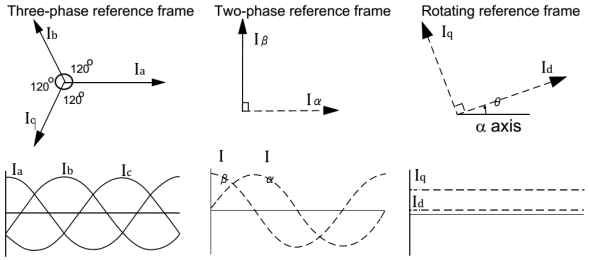


Figure 1.9
Varied coordinate axes



Prior to the above abc-dq axis conversion,owing to the fact that the voltage detected by the voltage detection circuit of three phase three wire circuit is line voltage (Vab, Vbc, Vca), the following conversion of line voltage to phase voltage (Line-abc to Phase-abc) is required to obtain the virtual phase voltage Van, Vbn and Vcn.

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \\ 0 & -1 & 1 \end{bmatrix}\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} \qquad (1.12)$$

Circuit Simulation

The circuit parameters of inverter

BUS Voltage V_{bus} = 100V

F_s = 20kHz，V_{tri} = 10V_{pp} (PWM)

C_{BUS} = 940uF，L = 1.02mH，C = 10uF

K_s = 0.3 (AC current sensing factor)

K_v = 1/60 (AC voltage sensing factor)

K_v = 1/40 (DC voltage sensing factor)

The analogue circuit diagram based on the parameters above is as the following figure 1.10 shown:

PSIM File: PEK-550_Sim1_3P_SVPWM_Inv(50Hz)_V11.1.5_V1.1

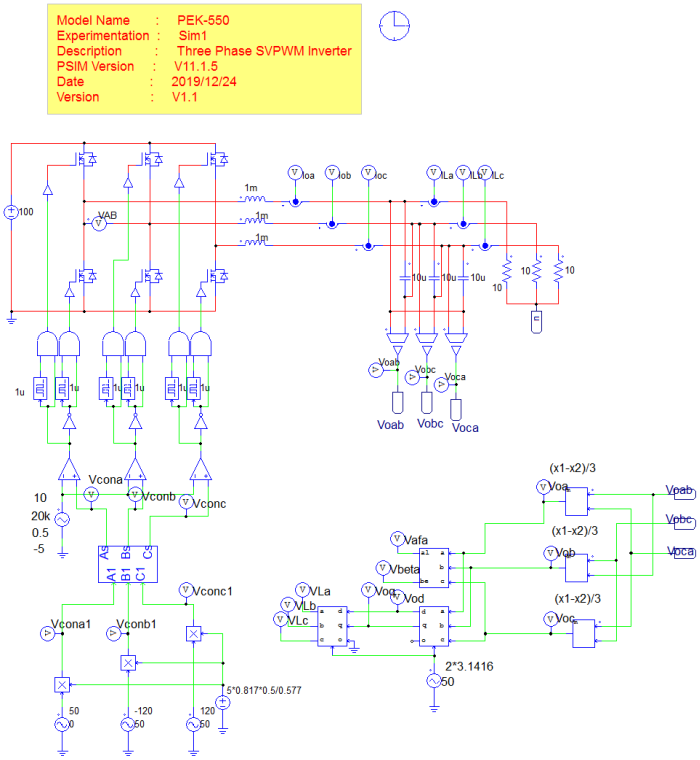


Figure 1.10 Experiment 1 PSIM analogue circuit diagram

The simulation result is shown within the figure 1.11 and 1.12:

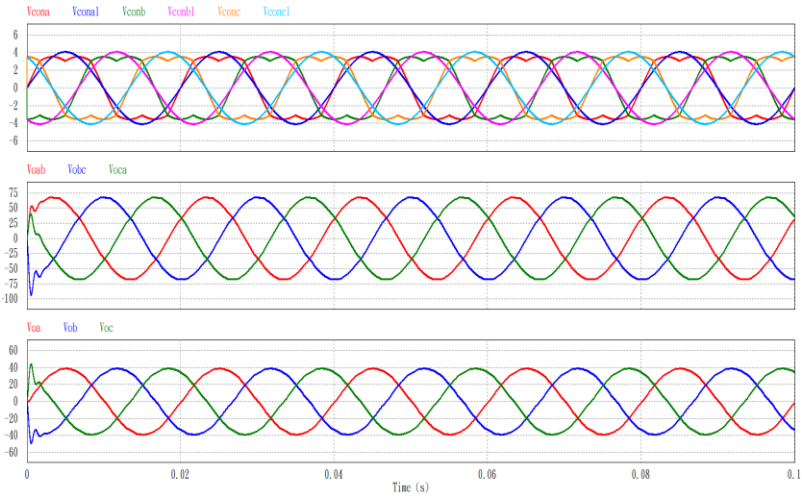


Figure 1.11 Experiment 1 analogue circuit simulation waveforms

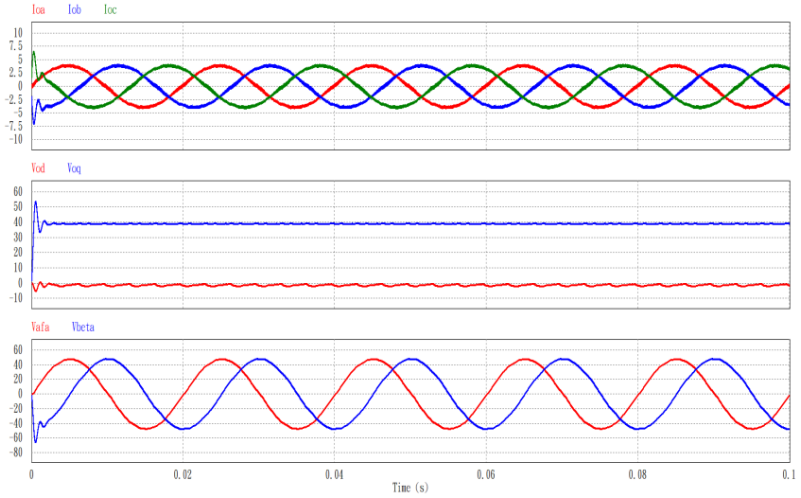


Figure 1.12 Experiment 1 analogue circuit simulation waveforms

The digital circuit diagram based on the analogue circuit is shown as the figure 1.13:
PSIM File: PEK-550_Lab1_3P_SVPWM_Inv(50Hz)_V11.1.5_V1.1

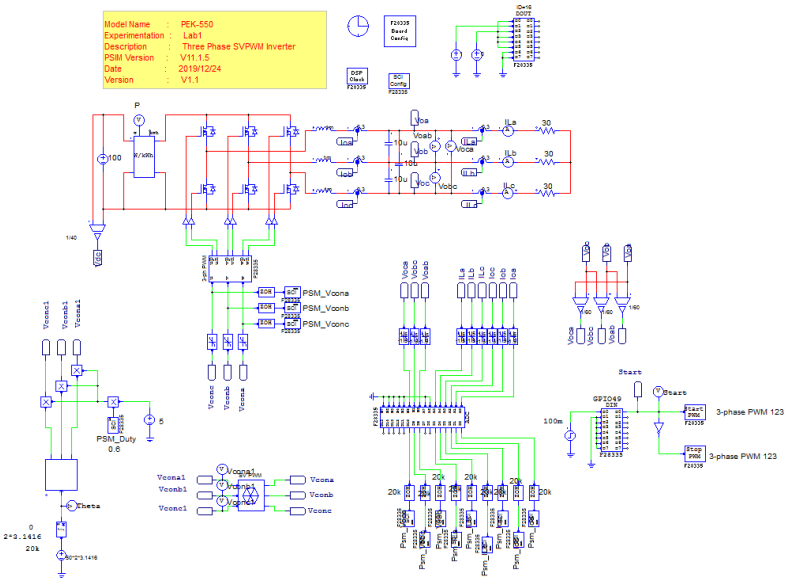


Figure 1.13 Experiment 1 digital circuit diagram

The simulation result is shown within the figure 1.14 and 1.15:

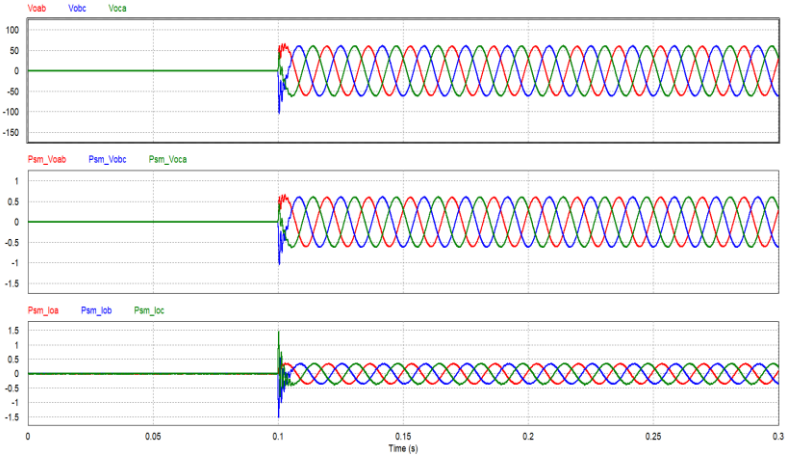


Figure 1.14 Experiment 1 digital circuit simulation waveforms

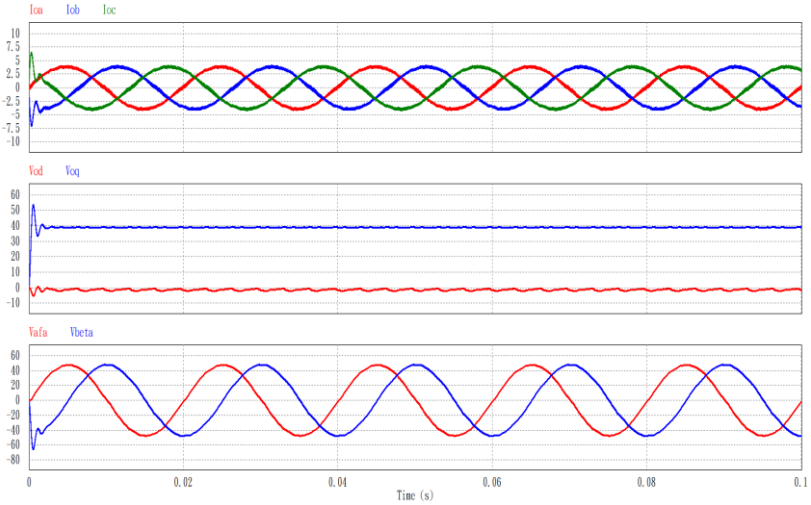


Figure 1.15 Experiment 1 digital circuit simulation waveforms

After confirming simulation, the corresponding C Code will be generated automatically via “Generate Code” of “Simulate”.

Experiment Devices

The required devices for experiment are as follows:

- PEK-540 * 1
- PEK-005A * 1
- PEK-006 * 1
- PTS-5000 * 1 (with GDS-2204E, PSW160-7.2 and GPL-500)
- PC * 1

Experiment Procedure

1. The experiment wiring is shown as the figure 1.16. Please follow it to complete wiring.

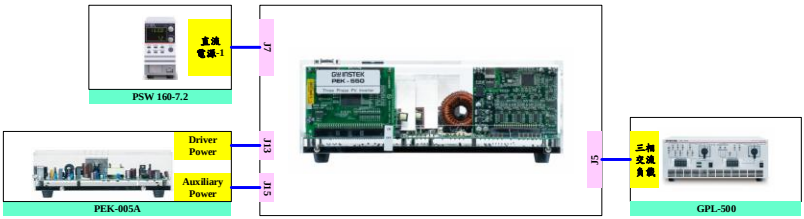


Figure 1.16 Experiment 1 wiring figure

2. After wiring, make sure the PEK-550 switch is OFF followed by turning the PEK-005A switch ON. The DSP red indicator lights on as the figure 1.17 shown, which means the DSP power is steadily normal.

Figure 1.17 DSP normal status with light on

3. Refer to the appendix B for burning procedure followed by referring to the appendix C for connection details.
4. Connect the test leads of oscilloscope to Vo-AB, Vo-BC, Vo-CA and Io-A, respectively, as the figure 1.18 shown.

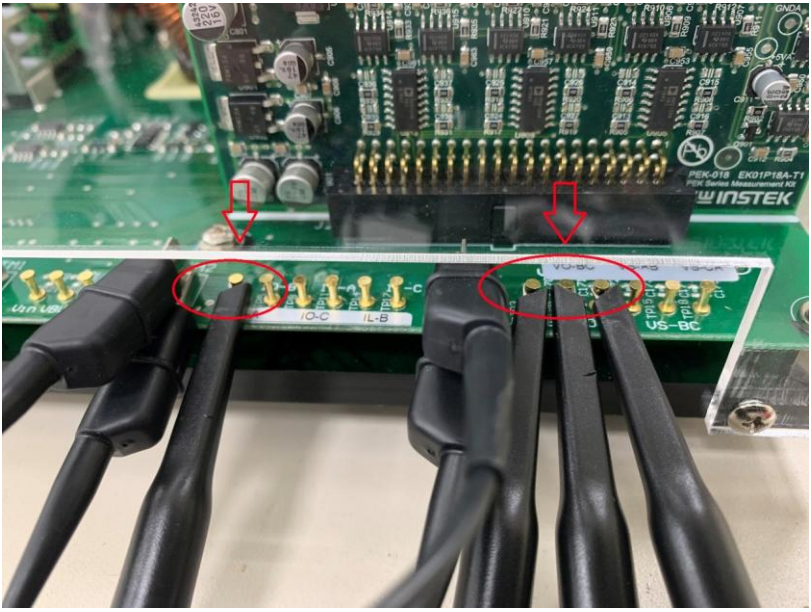


Figure 1.18 Oscilloscope test leads wiring

5. Set voltage 100V and current 3A for PSW 160-7.2 as the figure 1.9 shown.

Figure 1.9 The settings of PSW 160-7.2

6. As the figure 1.20 shown, follow the steps below for GPL-500 operation. Power on GPL-500 → Rotate the Three Phase Load knob to 2 (Resistance Load) → Set 1TS and 2TS as OFF, and 3TS as ON, which indicates no-load mode.

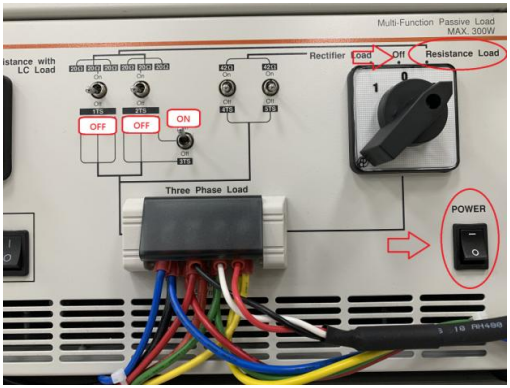


Figure 1.20 The no-load setting of GPL-500

7. After setting up and turning on PSW power output, finally turn on the switch of PEK-550.

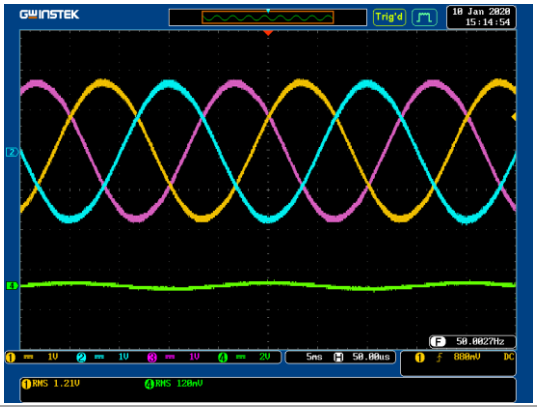
The purpose of experiment

(3) No Load

The figure 1.21 shows that when GPL-500 is set as no-load mode, Vo-AB output RMS voltage is 1.21V (42.16V in actual value), and Io-A is 0.12A (0.252A in actual value).

Figure 1.21

No-load measured waveform

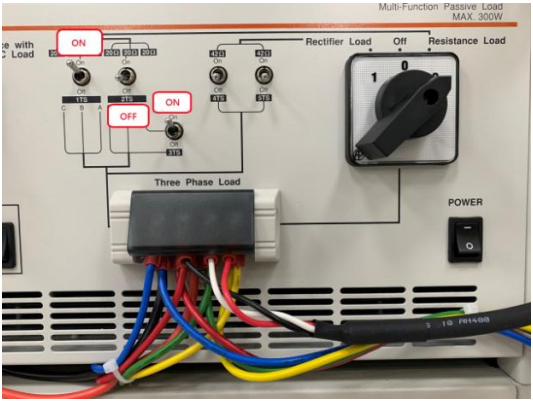


(4) Half Load (20Ω)

The figure 1.22 shows that 1Ts and 3TS are set ON, whereas 2TS is set OFF, which indicates half load.

Figure 1.22

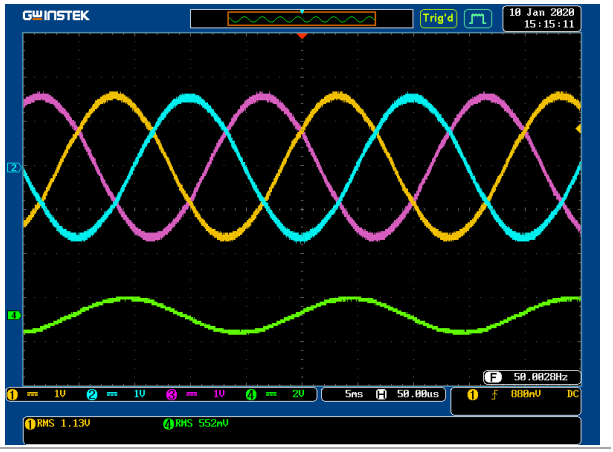
GPL-500 half-load setting



The figure 1.23 shows that when GPL-500 is set as half-load mode, Vo-AB output RMS voltage is 1.13V (39.373V in actual value), and Io-A is 0.55A (1.154A in actual value).

Figure 1.23

Half-load measured waveform

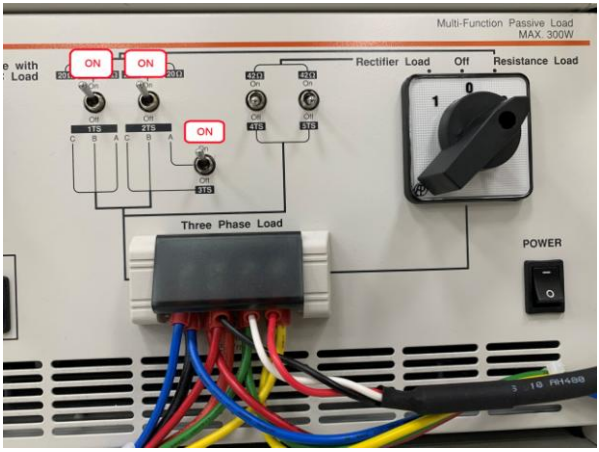


(5) Full Laod (10Ω)

The figure 1.24 shows that 1TS, 2TS and 3TS are set ON, which indicates full load.

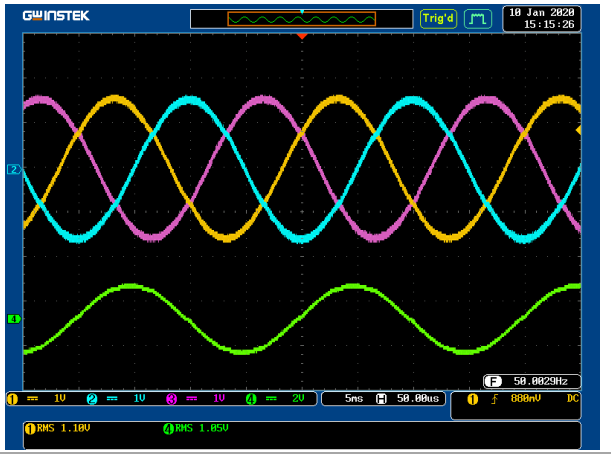
Figure 1.24

GPL-500 full-load setting



The figure 1.25 shows that when GPL-500 is set as full-load mode, Vo-AB output RMS voltage is 1.10V (38.328V in actual value), and Io-A is 1.05A (2.202A in actual value).

Figure 1.25 Full-load measured waveform



Per differed load operations, fill in the table 1.3 with the results in order. Refer to the table 0.1 for the sensing ratio.

Table 1.3 Output voltage current measured data in varied load settings

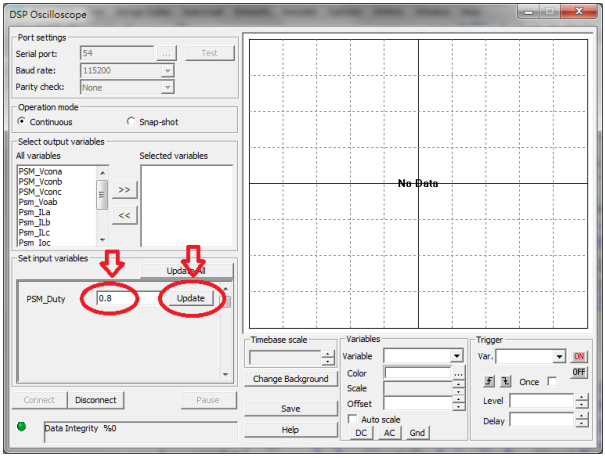
	Vo(Vrms) (Measured value)	Vo(Vrms) (Measured value)	Io(Arms) (Measured value)	Io(Arms) (Measured value)
N Load (no Load)	1.21V	42.16V	0.12A	0.252A
Half Load (20Ω)	1.13V	39.373V	0.55A	1.154A
Full Load (10Ω)	1.10V	38.328V	1.05A	2.202A

From the table 1.3, it is understandable that output voltage drops in accord with load increase uder open circuit condition.

Through the PSM_Duty, which is the Duty parameter within circuit, from the"Set input variables" adjusted by RS232, change the default 0.6 to 0.8 followed by pressing the Update as the figure 1.26 shown.

Figure 1.26

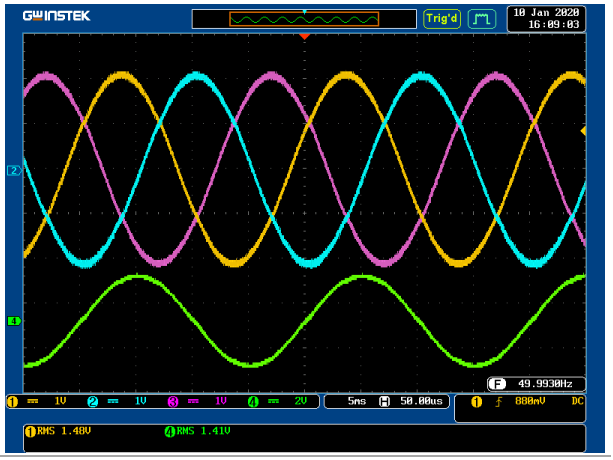
Duty adjustment



It is clear that output RMS voltage Vo-AB is changed from 1.10V (38.328V in actual value) to 1.48V (51.568V in actual value) as the figure 1.27 shown.

Figure 1.27

The measured waveform when Duty is 0.8



Per differed Duty operations, fill in the table 1.4 with the results in order. Refer to the table 0.1 for the sensing ratio.

Table 1.4 Output voltage current measured data in varied Duty settings

	Vo(Vrms) (Measured value)	Vo(Vrms) (Measured value)	Io(Arms) (Measured value)	Io(Arms) (Measured value)
Full Load Duty=0.6	1.10V	38.328V	1.05A	2.202A
Full Load Duty=0.8	1.48V	51.568V	1.41A	2.958A

From the table 1.4, it is clear that output voltage changes in accordance with Duty changes under open circuit condition.

Experiment 2 – Three Phase Boost Stand-alone Inverter

Preview

1. Learn the boost converter circuit model
2. Learn the boost converter circuit voltage current control and design
3. Learn the three phase inverter circuit model
4. Learn the three phase inverter voltage and current control and design
5. Learn how to establish analog circuit and simulation
6. Learn DSP digital control circuit planning

Purpose and Contents of Experiment

1. Observe output voltage fluctuations under vaired loads
2. Observe output voltage fluctuations under unbalanced load

Principle and Design

This experiment is the two-stage circuit with the first-stage boost converter and the second-class three phase three wire full-bridge inverter. The first stage is to maintain DC-link voltage, and the second-class is to control output voltage of inverter. The control architecture is as the figure 2.1 shown. We will illustrate each stage circuit respectively in this chapter.

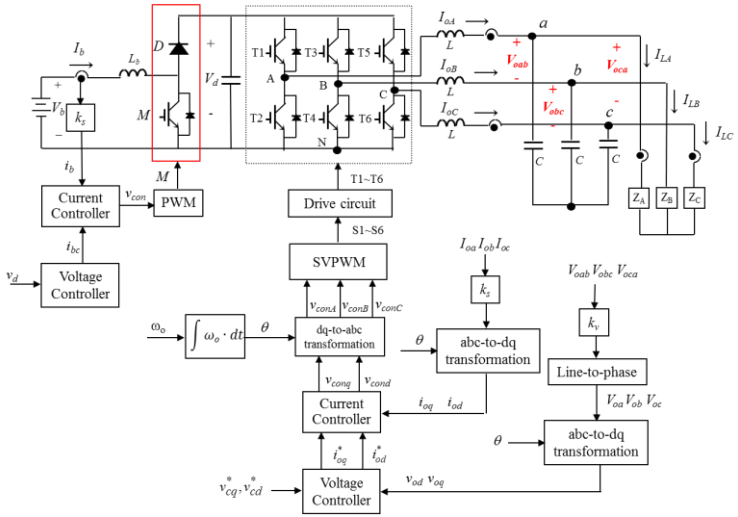


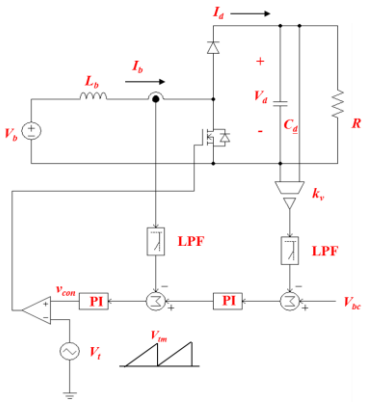
Figure 2.1 Diagram of full circuit control architecture

Boost Converter Controller Design

Refer to the figure 2.2 for the current mode control architecture of boost converter in which dual loop control is adopted and outer loop is voltage loop which is used to adjust voltage deviation and to generate current command of current inner loop. Current loop command and sensing current deviation can generate switchable drive signal via PWM. And sensing current is either, depending on the utilized control method, switchable current or inductance current. Basically, this experiment mainly focuses on average current control, for which we will explain below.

Figure 2.2

Current mode control architecture of boost converter



(6) Working Principle and Model Derivation

From the figure 2.2 we may obtain the follows via the status average method:

$$L_b \frac{dI_b}{dt} = V_b - (1-d)V_d \tag{2.1}$$

In which Duty indicates the follows:

$$d = \frac{v_{con}}{V_{tm}} \tag{2.2}$$

The following can be obtained via substitution:

$$L_b \frac{dI_b}{dt} = V_b - (1 - \frac{v_{con}}{V_{tm}})V_d \tag{2.3}$$

Also the following can be obtained via arrangement:

$$L_b \frac{dI_b}{dt} = \frac{V_d}{V_{tm}} v_{con} + V_b - V_d \tag{2.4}$$

And we further substitute $k_{pwmb} = \frac{V_d}{V_{tm}}$

$$L_b \frac{dI_b}{dt} = k_{pwmb}\, v_{con} + V_b - V_d \tag{2.5}$$

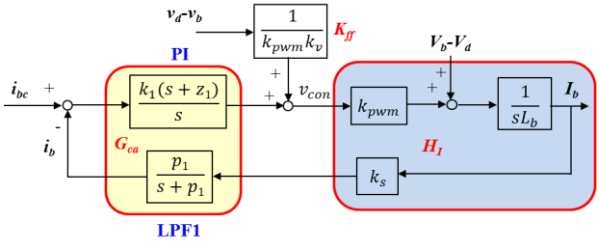
The equation (2.5) can be used to design current controller of boost converter.

Current Controller Design

Derived from the equation (2.5), the current loop control block is shown as the figure 2.3 in which Ks and Kv are voltage sensing gain and current sensing gain, individually, both of which adopt feedback control along with feedforward control methods to compensate the disturbance in current loop from Vb-Vd.

Figure 2.3

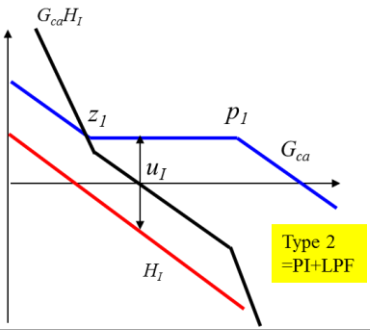
Current loop control block diagram



This current controller of circuit, known as the second-class error amplifier, can be divided into a Proportional Integration Controller (PI) and a Low Pass Filter (LPF). The bode plot is shown as the figure 2.4, of which the design method is illustrated below.

Figure 2.4

Current loop bode plot



1. Set u_I as 1/10~1/8 of change frequency.
2. Set z=u_I/3
3. Set p=f_s/2 (Low Pass Filter)
4. Obtain k1 via G_ca (u_I)H_I (u_I)=1

(7) Voltage Controller Design

In general, the response speed of voltage loop is way slower than that of current loop, so current loop is regarded as ideal when modeling voltage loop, which means the sensing inductance current along with the command response can be regarded as 1. Consequently, based on the previous assumption, voltage loop equivalent circuit can be simplified as the figure 2.5 shown. And the equation (2.6) is obtained from the figure 2.5.

$$\frac{V_b}{I_d} = R\frac{1+\frac{s}{\omega_z}}{1+\frac{s}{\omega_p}}, \quad \omega_z = \frac{1}{CR_e}, \quad \omega_p = \frac{1}{CR} \tag{2.6}$$

Substitute $I_d = k_b I_b$ into the previous equation to obtain $K_b = \frac{V_b}{V_d}$

$$\frac{V_b}{I_b} = R\frac{K_b(1+\frac{s}{\omega_z})}{1+\frac{s}{\omega_o}} \tag{2.7}$$

As the figure 2.6 shown, the control block diagram of voltage loop can be drawn, and the voltage error amplifier (Gea) can be designed, based on the previous second-class error amplifier, as the figure 2.7 shown. Therefore, voltage loop bandwidth can be designed at 1/3 ~ 1/5 of current loop bandwidth.

Figure 2.5

Voltage loop equivalent circuit

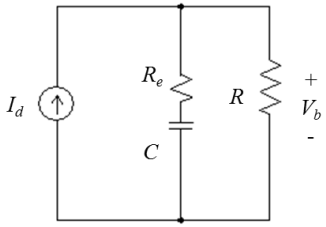


Figure 2.6

Current loop control block diagram

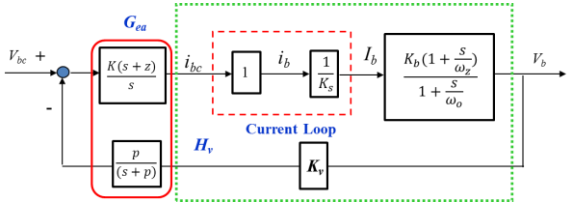
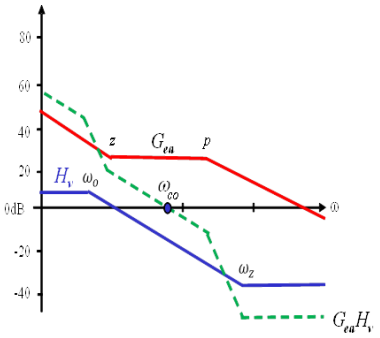


Figure 2.7
Voltage loop bode plot



Inverter Controller Design

The figure 2.8 describes three phase three wire inverter circuit where n is the virtual voltage neutral point and the control method adopts dual loop inductance current control. The following can be obtained via inverter circuit:

$$L\frac{dI_{oA}}{dt} = V_{AN} - V_{an} - V_{nN} \tag{2.8}$$

$$L\frac{dI_{oB}}{dt} = V_{BN} - V_{bn} - V_{nN} \tag{2.9}$$

$$L\frac{dI_{oC}}{dt} = V_{CN} - V_{cn} - V_{nN} \tag{2.10}$$

$$C\frac{dV_{an}}{dt} = I_{oA} - I_{LA} \tag{2.11}$$

$$C\frac{dV_{bn}}{dt} = I_{oB} - I_{LB} \tag{2.12}$$

$$C\frac{dV_{cn}}{dt} = I_{oC} - I_{LC} \tag{2.13}$$

Due to the fact that three wire circuit meets the follows:

$$I_{oA} + I_{oB} + I_{oC} = 0 \tag{2.14}$$

Via (2.14), the following can be obtained from (2.8)+(2.9)+(2.10):

$$V_{nN} = \frac{(V_{AN} + V_{BN} + V_{CN}) - (V_{an} + V_{bn} + V_{cn})}{3} \tag{2.15}$$

The following can be obtained via substituting (2.15) into (2.8)~(2.10):

$$\begin{bmatrix} L\frac{dI_{oA}}{dt} \\ L\frac{dI_{oB}}{dt} \\ L\frac{dI_{oC}}{dt} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ -\frac{1}{2} & 1 & -\frac{1}{2} \\ -\frac{1}{2} & -\frac{1}{2} & 1 \end{bmatrix}\left(\begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \end{bmatrix} - \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix}\right) \tag{2.16}$$

$$\begin{bmatrix} I_{capa} \\ I_{capb} \\ I_{capc} \end{bmatrix} = \begin{bmatrix} C\frac{dV_{an}}{dt} \\ C\frac{dV_{bn}}{dt} \\ C\frac{dV_{cn}}{dt} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} I_{oA} \\ I_{oB} \\ I_{oC} \end{bmatrix} - \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} I_{LA} \\ I_{LB} \\ I_{LC} \end{bmatrix} \tag{2.17}$$

V_{iN} (i=A, B, C) is the output voltage of A, B and C arms. Generally, the control method inverter usually adopts is three phase sinusoidal PWM (SPWM) where each arm of three phase employs the control voltage (v_{conA}、v_{conB}、v_{conC}) of phase shift 120 degree, which compares with triangle wave (v_{tri}) individually in order to trigger switch of three arms. The output voltage of each arm can be described as the following (2.18) shown:

$$V_{iN} = (\frac{1}{2} + \frac{V_{coni}}{2v_{tm}})V_d \ (i=A, B, C) \tag{2.18}$$

Where v_{tm} indicates the amplitude of triangle wave and (2.19) can be obtained via substituting (2.18) into (2.16).

$$\begin{bmatrix} L\frac{dI_{oA}}{dt} \\ L\frac{dI_{oB}}{dt} \\ L\frac{dI_{oC}}{dt} \end{bmatrix} = \frac{V_d}{3v_{tm}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ -\frac{1}{2} & 1 & -\frac{1}{2} \\ -\frac{1}{2} & -\frac{1}{2} & 1 \end{bmatrix} \begin{bmatrix} V_{conA} \\ V_{conB} \\ V_{conC} \end{bmatrix} - \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ -\frac{1}{2} & 1 & -\frac{1}{2} \\ -\frac{1}{2} & -\frac{1}{2} & 1 \end{bmatrix} \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} \quad (2.19)$$

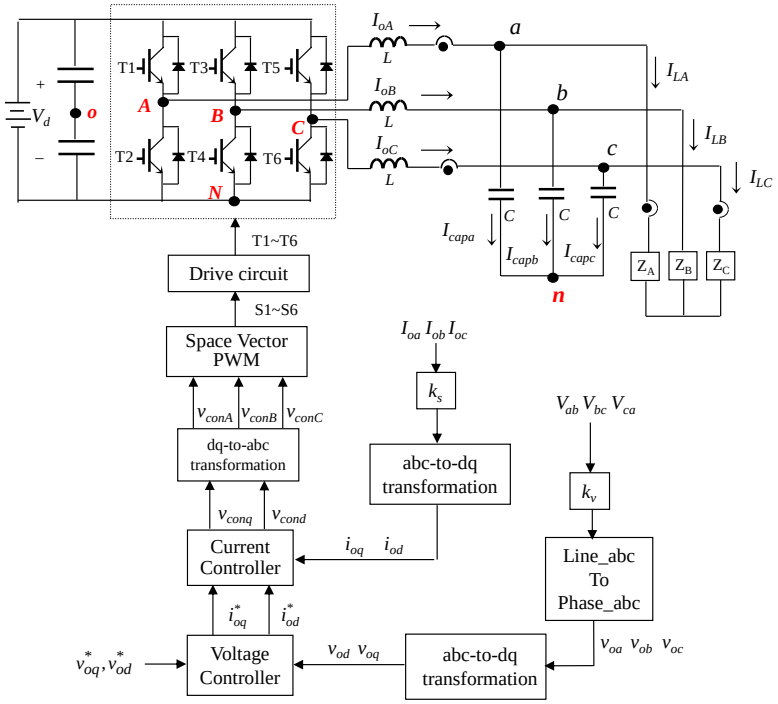


Figure 2.8 Three phase three wire inverter

Axis Conversion

We can understand, from the relation of each phase current and three phase SPWM control voltage derived from the eqution (2.19), that each phase current control is not only affected by the corresponding control voltage, but also affected by control voltage of other phases. That is, each phase current control hasn't been decoupled. If designing controller from the abc static frame directly under the three phase unbalanced condition, each phase will influence one another and thus the control function will be affected. In order to overcome the previous issue, we usually adopt the method of coordicate axis conversion which decouples mathematical model logically as the figure 2.9 shown where three coordinate axes (a, b, c) represent a static frame, which indicates components of phase current and phase voltage from three phase

inverter, whereas a, b represent the static frame of two phase that transforms three phase with 120 degree difference of each phase AC volume into two phases with 90 degree difference of each phase AC volume. The d, q axes and zero axis are synchronous rotating coordinate. Under the condition of three phase balanced, zero axis volume is zero, which can be simplified into vertical dq two axes. The formula of three phase abc static coordinate axis and two phase dq0 synchronous rotating coordinate axis is as follows:

$$\begin{bmatrix} f_d \\ f_q \\ f_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos\theta & \cos(\theta-\frac{2\pi}{3}) & \cos(\theta+\frac{2\pi}{3}) \\ \sin\theta & \sin(\theta-\frac{2\pi}{3}) & \sin(\theta+\frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \quad (2.20)$$

$$\begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta & 1 \\ \cos(\theta-\frac{2\pi}{3}) & \sin(\theta-\frac{2\pi}{3}) & 1 \\ \cos(\theta+\frac{2\pi}{3}) & \sin(\theta+\frac{2\pi}{3}) & 1 \end{bmatrix}\begin{bmatrix} f_d \\ f_q \\ f_0 \end{bmatrix} \quad (2.21)$$

In which:

$$\theta = \omega t \quad (2.22)$$

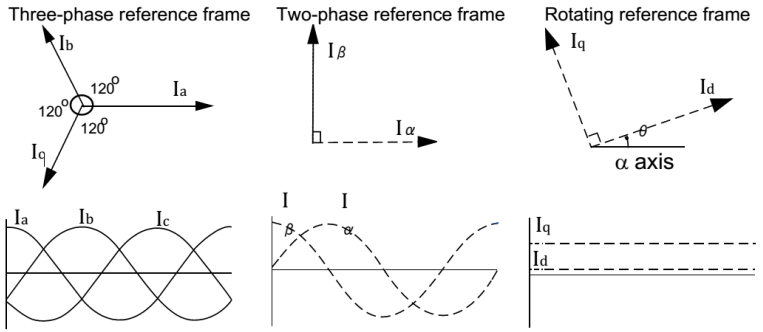


Figure 2.9 Several coordinate axes

The state equation of three phase three wire inverter as the figure 2.8 shown can be inferred from substituting axis conversion formula of (2.20) and (2.21) for (2.17) and (2.19).

$$\begin{bmatrix} L\frac{dI_{od}}{dt} \\ L\frac{dI_{oq}}{dt} \\ L\frac{dI_{o0}}{dt} \end{bmatrix} = \frac{V_d}{2V_{tm}} \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{cond} \\ V_{conq} \\ V_{con0} \end{bmatrix} - \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{od} \\ V_{oq} \\ V_{o0} \end{bmatrix} - \begin{bmatrix} 0 & \omega L & 0 \\ -\omega L & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{od} \\ I_{oq} \\ I_{o0} \end{bmatrix} \quad (2.23)$$

$$\begin{bmatrix} C\frac{dV_{od}}{dt} \\ C\frac{dV_{oq}}{dt} \\ C\frac{dV_{o0}}{dt} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} I_{od} \\ I_{oq} \\ I_{o0} \end{bmatrix} - \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} I_{od} \\ I_{oq} \\ I_{o0} \end{bmatrix} - \begin{bmatrix} 0 & \omega C & 0 \\ -\omega C & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{od} \\ V_{oq} \\ V_{o0} \end{bmatrix} \quad (2.24)$$

Vconi(i=d, q) is dq axis PWM control voltage, whilst Vtm is PWM triangle amplitude.

Prior to the above abc-dq axis conversion, due to the fact that the voltage detected by voltage detection circuit of three phase three wire circuit is line voltage (Vab, Vbc, Vca), the line voltage to phase voltage conversion (Line-abc to Phase-abc) is required to obtain the virtual phase voltage of Van, Vbn and Vcn from (2.19).

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \\ 0 & -1 & 1 \end{bmatrix} \begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} \quad (2.25)$$

Currrent Controller Design

As the figure 2.10 shown, the inverter current controller can be designed via equation (2.23) where currents of both d and q axes cause perturbation on another axis and thus the perturbation are eliminated by the figure 2.10 via feedforward control signal vff2. The other feedforward control signal vff1 is used to erase the perturbation from same phase output voltage to current loop. The kv and ks are voltage sensing gain and current sensing gain

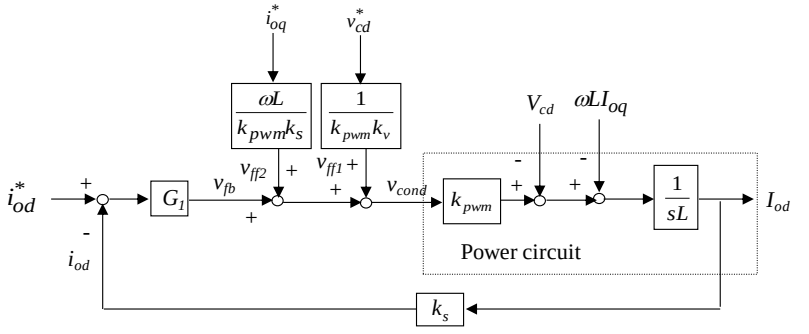
individually. The current deviation amplifier G can be designed by P, PI or the second-class deviation amplifier. If adopting P control (GI=k1), the current loop response can be obtained via current feedback loop as follows:

$$\frac{i_{o,i}^{*}}{i_{o,i}} = \frac{\frac{k_{pwm}k_s k_1}{L}}{s + \frac{k_{pwm}k_s k_1}{L}} = \frac{u_I}{s + u_I} \quad ,i = d,\ q \tag{2.26}$$

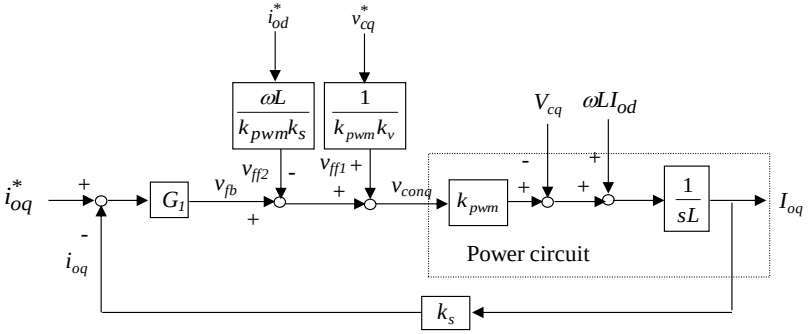
The uI indicates current loop bandwidth as follows:

$$u_I = \frac{k_{pwm}k_s k_1}{L} \tag{2.27}$$

The bandwidth can be set up by gain k1 of current deviation amplifier.



(a)

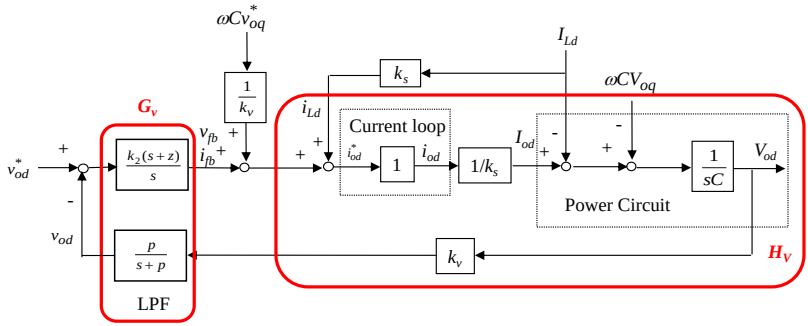


(b)

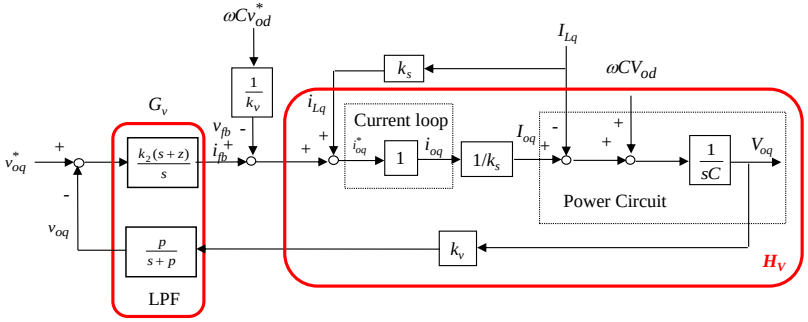
Figure 2.10 Inverter current control loop: (a) d axis, (b) q axis

(8) Voltage Controller Design

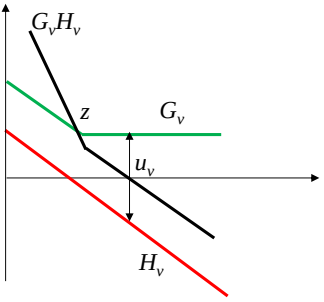
The inverter voltage loop control block diagram is shown as the figure 2.11 where electric circuit block is drawn via equation (2.24). If bandwidth (uI) of current loop response is larger than that of voltage loop by 4 times, current loop response equation (2.26), while analyzing voltage loop response, can be regarded as 1. The voltage controller adopts both feedforward control and feedback control. Due to the sensing load current, the controller directly eliminates the perturbation on voltage loop from load current via the sensing load current added into current command. Also, it utilizes voltage command (vod* and voq*) multiplying by ωC with adding current command from another axis to eliminate perturbation of capacitor current (ωCVod and ωCVoq). The voltage feedback controller Gv, known as the second-class deviation amplifier, is composed of a feedback proportional integrator controller and a low pass filter (LPF) of voltage feedback signal. The voltage loop bode plot is shown as the figure 2.11(c) where voltage loop bandwidth, generally, is placed at the ¼ of current loop bandwidth. In order to gain perfect voltage adjustion rate and three phase voltage balance under the three phase load unbalanced condition, each line voltage is supposed to be adjusted RMS value, respectively. This experiment, based on the voltage RMS value controller from the figure 2.12, calculates three output line voltage RMS values (vabm, vbcm, vcam) individually followed by comparing with RMS value command and resulting in, after Gm adjustion, an amplitude corrected signal (Am1 Am2, Am3), which is used to correct the original line voltage amplitude command Am0. Finally, the obtained line voltage amplitude command Amab, Ambc, Amca multiplies by three phase sine wave $\sin(\omega t+\pi/6)$, $\sin(\omega t-\pi/2)$ and $\sin(\omega t+5\pi/6)$ of virtual phase voltage phase shift through 30 degree to obtain the transient voltage command of three phase line voltage. After that, via Line-abc to Phase-abc conversion and abc-dq axis conversion, the ultimate voltage loop command vod* and voq* is thus generated.



(a)



(b)



(c)

Figure 2.11 Inverter voltage control loop: (a) d axis，(b) q asix，(c) voltage loop bode plot

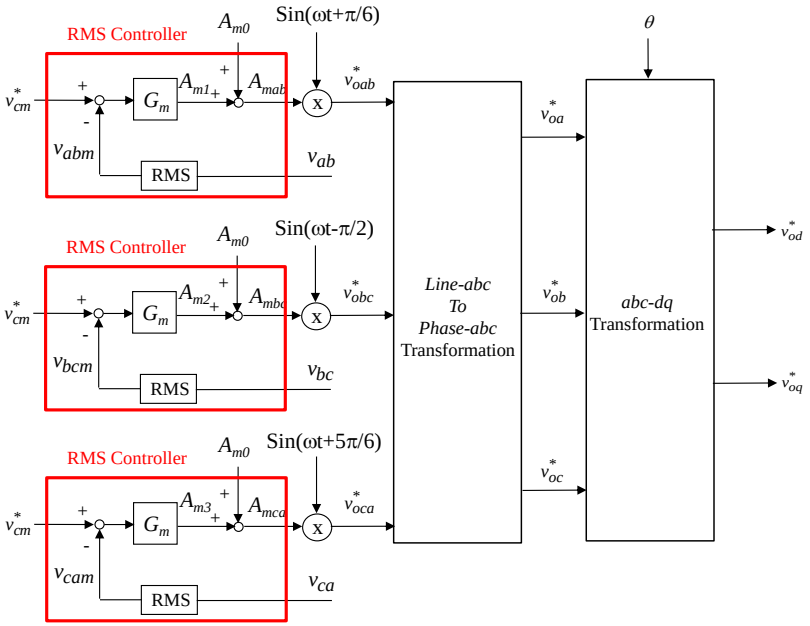


Figure 2.12 Voltage RMS value controller

Circuit Simulation

The circuit parameters of converter are as follows:

The inverter specification	DC Input Voltage Vb = 70V
	DC Bus Voltage Vd= 100V
	Fs = 40kHz, Vtri = 5Vpp (Boost PWM)
	Fs = 20kHz, Vtri = 10Vpp (Inverter PWM)
	C_b = 200uF, L_b = 660uH
	C_{BUS} = 940uF, L = 1.02mH, C = 10uF
	Ks = 0.3 (AC current sensing factor)
	Ks = 0.6 (DC current sensing factor)
	Kv = 1/60 (AC voltage sensing factor)
	Kv = 1/40 (DC voltage sensing factor)

The analogue circuit diagram based on the parameters above is as the following figure 2.13 shown:
PSIM File: PEK-550_Sim2_3P_Boost_SA_Inv(50Hz)_V11.1.5_V1.1

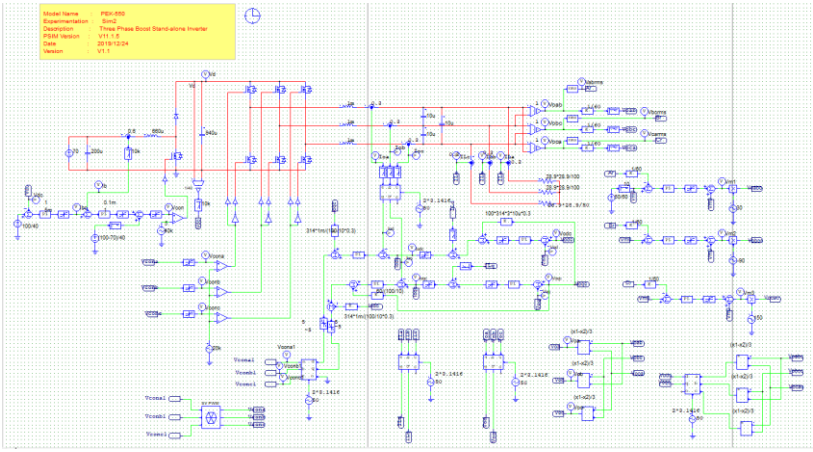


Figure 2.13 Experiment 2 PSIM analogue circuit diagram

The simulation result is shown within the figure 2.14 and 2.15:

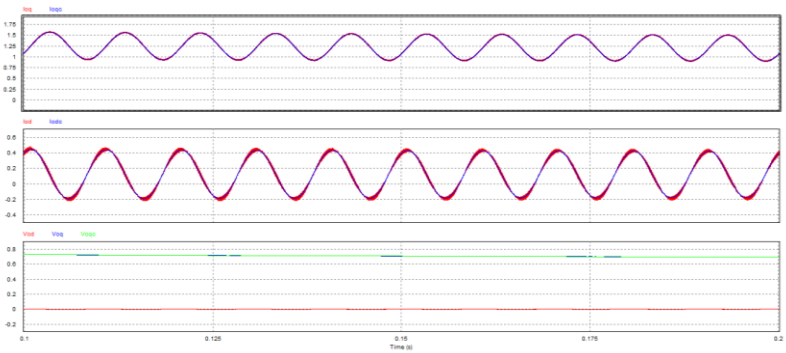


Figure 2.14 Experiment 2 analogue circuit simulation waveforms

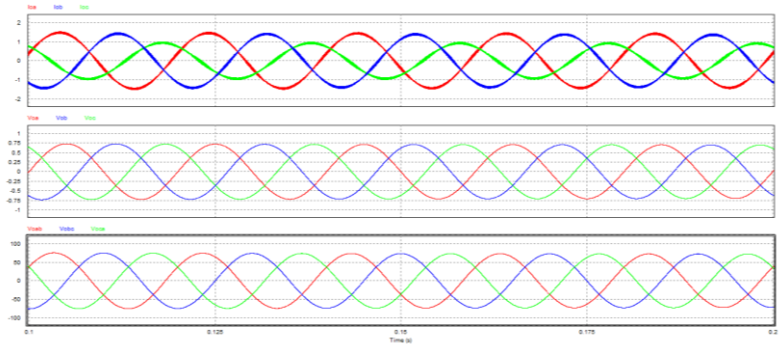


Figure 2.15 Experiment 2 analogue circuit simulation waveforms

The digital circuit diagram based on the analogue circuit is shown as the figure 2.16:
PSIM File: PEK-550_Lab2_3P_Boost_SA_Inv(50Hz)_V11.1.5_V1.1

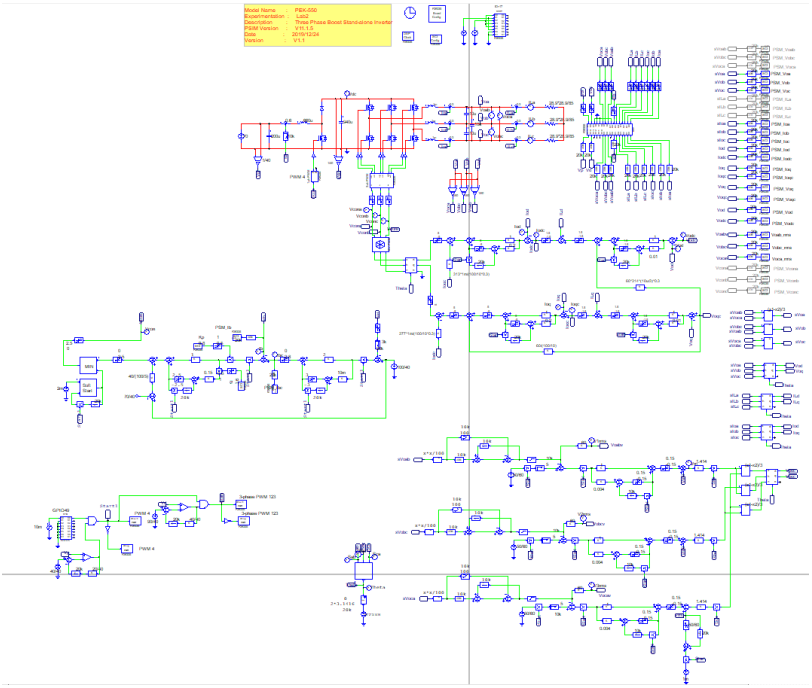


Figure 2.16 Experiment 2 PSIM digital circuit diagram

The simulation result is shown within the figure 2.17 and 2.18:

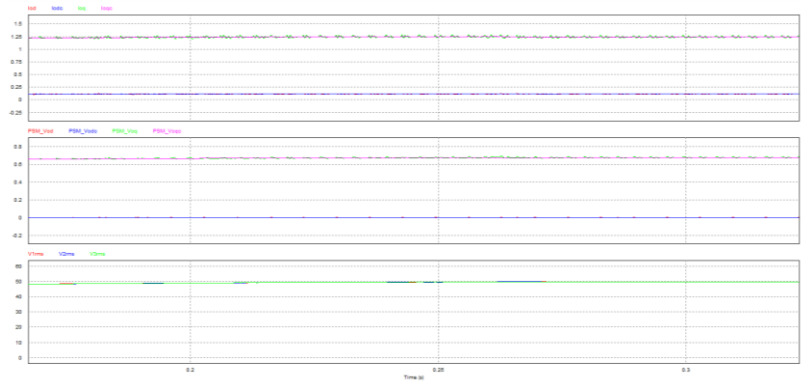


Figure 2.17 Experiment 2 digital circuit simulation waveforms

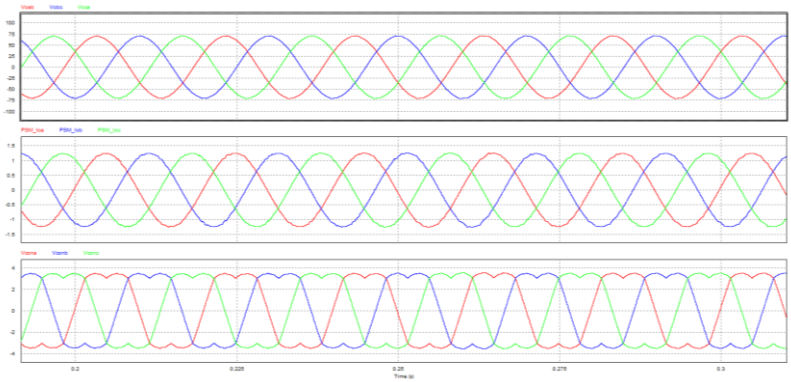


Figure 2.18 Experiment 2 digital circuit simulation waveforms

After confirming simulation, the corresponding C Code will be generated automatically via “Generate Code” of “Simulate”.

Experiment Devices

The required devices for experiment are as follows:

- PEK-550 * 1
- PEK-005A * 1
- PEK-006 * 1
- PTS-5000 * 1 (with GDS-2204E, PSW160-7.2 and GPL-500)
- PC * 1

Experiment Procedure

1. The experiment wiring is shown as the figure 2.19. Please follow it to complete wiring.

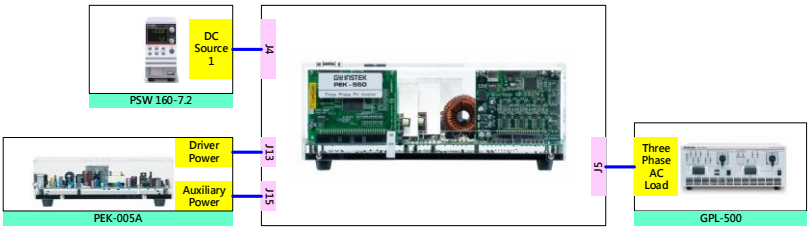


Figure 2.19 Experiment 2 wiring figure

2. After wiring, make sure the PEK-550 switch is OFF followed by turning the PEK-005A switch ON. The DSP red indicator lights on as the figure 2.20 shown, which means the DSP power is steadily normal.

Figure 2.20 DSP normal status with light on

3. Refer to the appendix B for burning procedure.
4. Connect the test leads of oscilloscope to Vo-AB, Vo-BC, Vo-CA and Io-A, respectively, as the figure 2.21 shown.

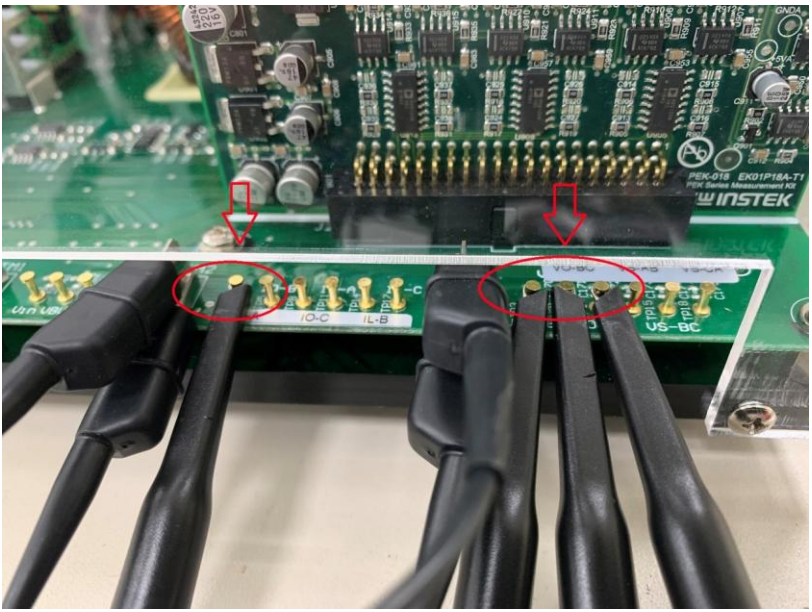


Figure 2.21 Oscilloscope test leads wiring

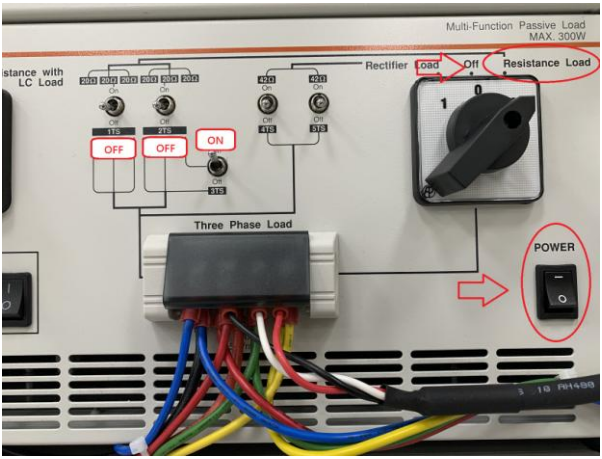
5. As the figure 2.22 shown, set voltage as 70V and current as 5A, individually, for the power supply PSW160-7.2.

Figure 2.22 The settings of PSW 160-7.2

6. After powering on GPL-500, set Resistance Load for Three Phase Load. Further set 1TS and 2TS as OFF and 3TS as ON, which indicates no load as the figure 2.23 shown.

Figure 2.23

GPL-500 no-load setting



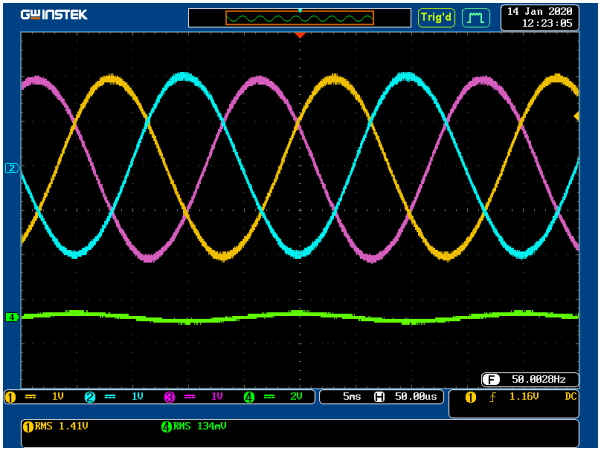
7. After setting up and turning on PSW power output, finally turn on PEK-550.

The purpose of experiment

(1) No Load

Under the condition of no-load, the figure 2.24 shows that Vo-AB output RMS voltage is 1.41V (49.129V in actual value), and Io-A is 0.13A (0.273A in actual value).

Figure 2.24 No-load measured waveforms



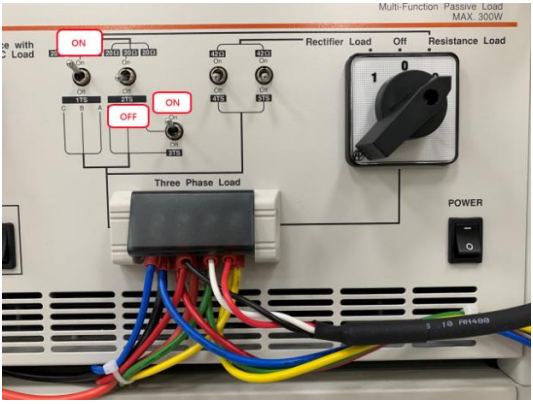
$V_{o_{ab}}$: $CH1(yellow)$: 1V/div $V_{o_{ca}}$: $CH3$(purple): 1V/div

$V_{o_{bc}}$: $CH2(blue)$: 1V/div I_{o_a} : $CH4$(green): 2V/div

(2) Half Load (20Ω)

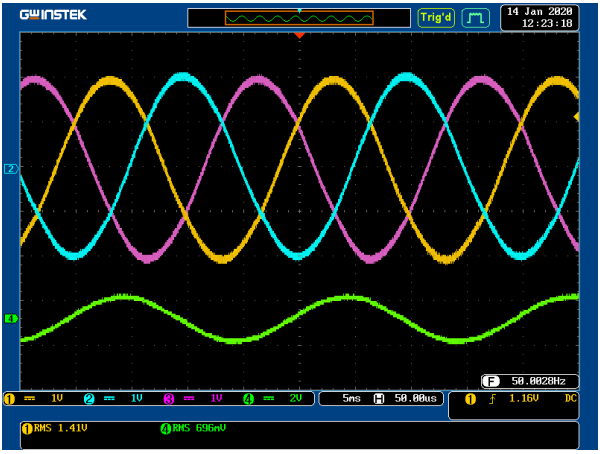
The figure 2.25 shows that 1TS and 3TS are set ON, whilst 2TS is set OFF, which indicates half load.

Figure 2.25
GPL-500 half-load setting



Under the condition of half-load, the figure 2.26 shows that Vo-AB output RMS voltage is 1.41V (49.129V in actual value), and Io-A is 0.696A (1.46A in actual value).

Figure 2.26
Half-load measured waveforms



$V_{o_{ab}}$: $CH1(yellow)$: 1V/div $V_{o_{ca}}$: $CH3$(purple): 1V/div

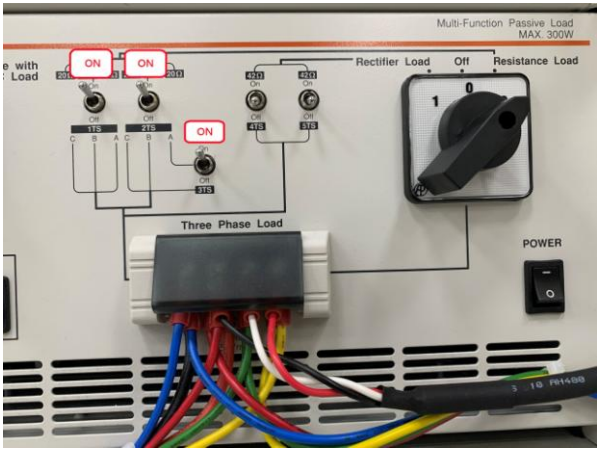
$V_{o_{bc}}$: $CH2(blue)$: 1V/div I_{o_a} : $CH4$(green): 2V/div

(3) Full Load (10Ω)

The figure 2.27 shows that 1TS, 2TS and 3TS are set ON, which indicates full load.

Figure 2.27

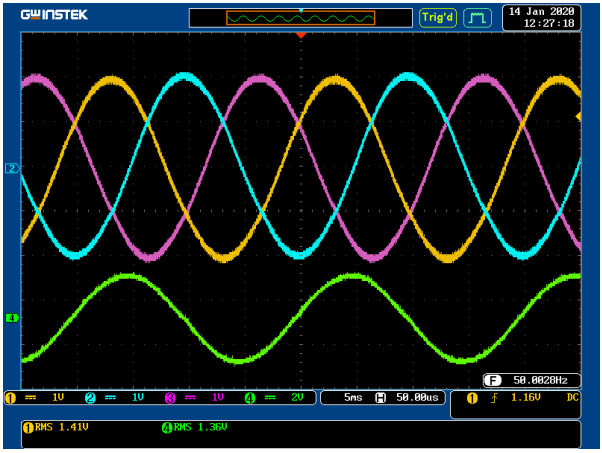
GPL-500 full-load setting



Under the condition of full-load, the figure 2.28 shows that Vo-AB output RMS voltage is 1.41V (49.129V in actual value), and Io-A is 1.36A (2.852A in actual value).

Figure 2.28

Full-load measured waveforms



$V_{o_{ab}}$: $CH1(yellow)$: 1V/div $V_{o_{ca}}$: $CH3$(purple): 1V/div

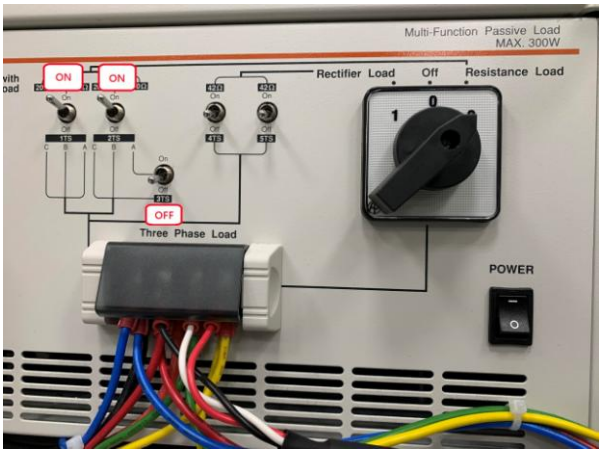
$V_{o_{bc}}$: $CH2(blue)$: 1V/div I_{o_a} : $CH4$(green): 2V/div

(4) Unbalanced Load (A phase 20Ω, B and C phase 10Ω)

The figure 2.29 shows that 1TS and 2TS are set ON, whilst 3TS is set OFF, which indicates unbalanced load.

Figure 2.29

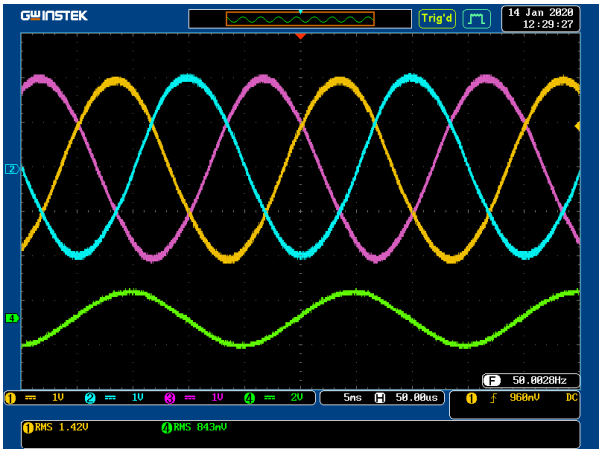
GPL-500 unbalanced-load setting



Under the condition of unbalanced load, the figure 2.30 shows that Vo-AB output RMS voltage is 1.41V (49.129V in actual value), and Io-A is 0.83A (1.741A in actual value), and Io-B is 1.24A (2.601A in actual value), and Io-C is 1.22A (2.559A in actual value).

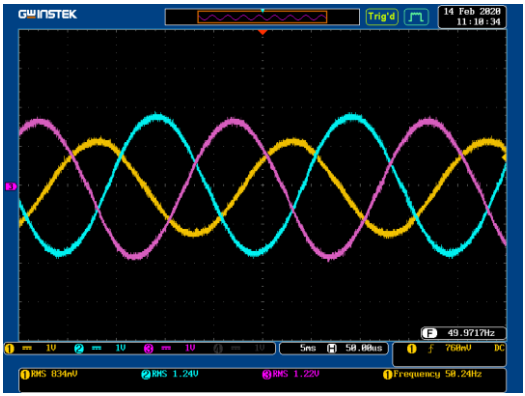
Figure 2.30

Unbalanced load measured waveforms



$V_{o_{ab}}$: $CH1(yellow)$: 1V/div $V_{o_{ca}}$: $CH3$(purple): 1V/div

$V_{o_{bc}}$: $CH2(blue)$: 1V/div I_{o_a} : $CH4$(green): 2V/div



I_{o_A} : $CH1(yellow)$: 1V/div I_{o_C} : $CH3$(purple): 1V/div

I_{o_B} : $CH2(blue)$: 1V/div

Per differed load operations, fill in the table 2.1 with the measured results in order. Refer to the table 0.1 for the sensing ratio.

Table 2.1 Output voltage current measured data in varied load settings

	Vo(Vrms) (Measured value)	Vo(Vrms) (Measured value)	Io(Arms) (Measured value)	Io(Arms) (Measured value)
No Load	1.41V	49.129V	0.13A	0.273A
Half Load (20Ω)	1.41V	49.129V	0.70A	1.46A
Full Load (10Ω)	1.41V	49.129V	1.36A	2.852A
Unbalanced Load				
RA=20Ω	1.41V	49.129V	0.83A	1.741A
RB=10Ω			1.24A	2.601A
RC=10Ω			1.22A	2.559A

From the table 2.1 we may understand that output voltage will not change in accordance with load fluctuation under the condition of closed loop.

Experiment 3 – Three Phase Grid-connected Inverter

Preview

1. Learn three phase grid-connected inverter circuit model
2. Learn dual closed-loop DC voltage and current controller design of three phase grid-connected inverter
3. Learn phase-lock loop control
4. Learn analog circuit establishment and simulation
5. Learn DSP digital control circuit planning

Experiment Purpose and Contents

1. Get familiar with grid power operation of three phase grid-connected inverter
2. Observe system power fluctuation via load change after grid power establishment.

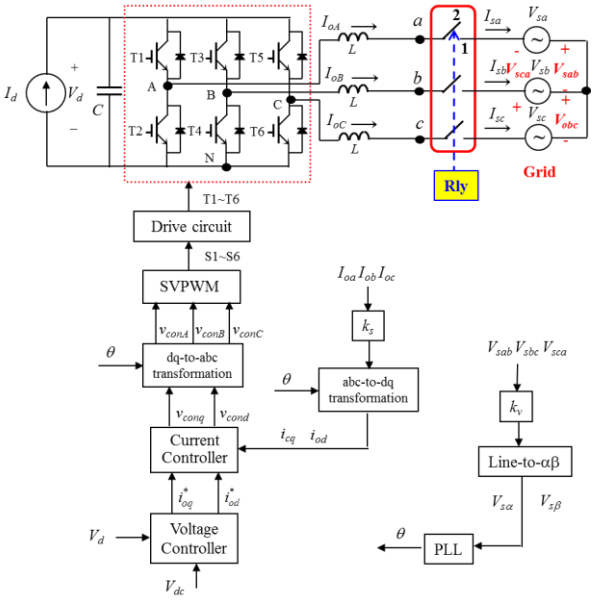
Principle and Design

Three phase grid power parallel circuit inverter, which is required by several renewable energy power system, energy storage system, and grid power interface, among others, contains multi-level circuits. The experiment puts emphasis upon grid power parallel circuit inverter control and therefore the circuit architecture is simplified to only inverter part as the figure 3.1 shown in which

input current Id indicates the current generated by the previous stage circuit. The inverter per se adopts dual loop control; outer loop is DC voltage control loop, whilst inner loop is inductance current control loop. In addition, the current of inverter grid power synchronizes with the voltage of grid power, and thus needs a phase-lock loop control (Phase Lock Loop, PLL).

Figure 3.1

Three phase grid power parallel circuit inverter control architecture



Current Loop Design

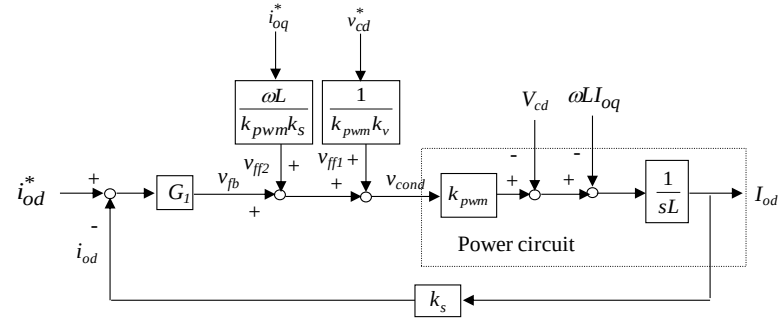
The equivalent circuit model of three phase grid power parallel circuit inverter, which is identical with the previous Lab 2 individual inverter model, is able to transform circuit to synchronous rotating frame, via abc-dq axis conversion, in order to simplify controller design. The current controller of inverter under dq axis is shown as the figure 3.2 where currents of d and q axes impose perturbation on the current loop of another axis. Therefore, the figure 3.2 eliminates the perturbation via feedforward control signal vff2. And the other feedforward control signal vff1 is used to eliminate the perturbation from the same phase output voltage to current loop. The kv and ks are voltage and current sensing gain, respectively. The current deviation amplifier GI can be designed via adopting P, PI or the second-class deviation amplifier. If adopting P control (GI=k1), the current loop response can be obtained as follows via current feedback loop.

$$\frac{i_{o,i}^{*}}{i_{o,i}} = \frac{\frac{k_{pwm}k_s k_1}{L}}{s + \frac{k_{pwm}k_s k_1}{L}} = \frac{u_I}{s + u_I} \quad ,i = d, q \tag{3.1}$$

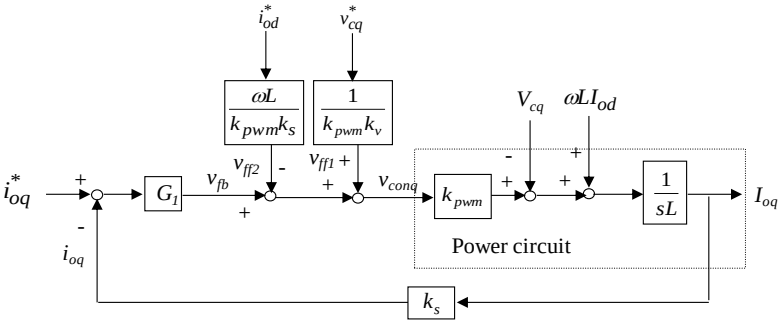
The uI indicates current loop bandwidth:

$$u_I = \frac{k_{pwm}k_s k_1}{L} \tag{3.2}$$

It can be designed via gain k1 of current deviation amplifier.



(a)



(b)

Figur 3.2 Inverter current control loop: (a)d axis, (b)q axis

Voltage Loop Design

The purpose of DC voltage control is to maintain power balance; that is, the power transmited from front-end circuit is in balance with the power fed in grid power from inverter. Therefore, after removing steady state DC working point, the equivalent small signal circuit model of voltage loop can be shown as the figure 3.3 (a); that is, inverter is regarded as a small signal of current source Id which charges to DC capacitor.

AC side transient power is described as follows:

$$P_{ac} = \mathrm{V}_{\alpha}\mathrm{I}_{\alpha} + \mathrm{V}_{\beta}\mathrm{I}_{\beta} = \mathrm{V}_{s(p)} \sin \omega t \cdot Im \sin \omega t + V_{s(p)} \cos \omega t \cdot Im \cos \omega t \quad (3.3)$$

$V_{s(p)}$ is dq axis peak value voltage, whereas I_m is dq axis peak value current. The equation can be simplified as follows via the above trigonometric functions:

$$P_{ac} = V_{s(p)} I_m \quad (3.4)$$

The figure 3.3 (b) shows that current source responses to DC side. If inverter efficiency is 100%, the input power P_{ac} will be equivalent with output power P_{dc}.

$$P_{dc} = P_{ac} \quad (3.5)$$

In addition, DC side power can be expressed as follows:

$$P_{dc} = V_d I_d \quad (3.6)$$

Therefore

$$V_d I_d = V_{s(p)} I_m \quad (3.7)$$

$$I_d = \frac{V_{s(p)} I_m}{V_d} = K_{dc} I_m \quad (3.8)$$

$$\tilde{V}_d = \tilde{I}_d \frac{1}{sC} \quad (3.9)$$

From the figure 3.3 (b), the transfer function of DC side current source to DC voltage is shown as follows:

$$\frac{\tilde{V}_d}{\tilde{I}_m} = \frac{K_{dc}}{sC}, \quad K_{dc} = \frac{V_{s(p)}}{V_d} \quad (3.10)$$

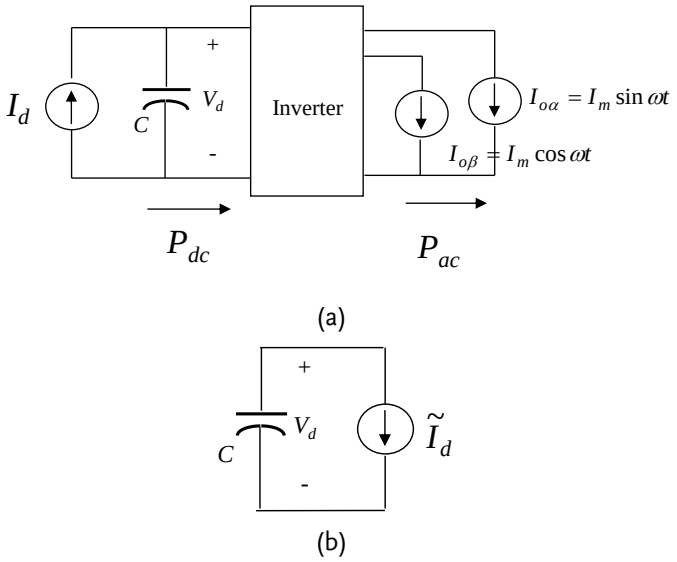


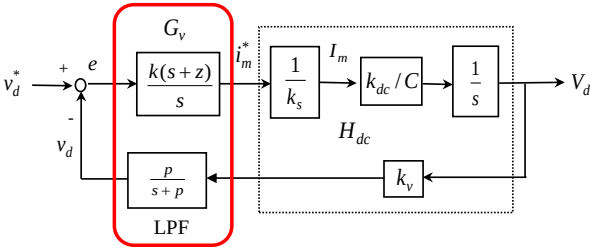
Figure 3.3 Voltage loop: (a) dq axis equivalent circuit, (b) transferred to DC side equivalent circuit

In light with the equation (3.8), the designed DC voltage control block diagram is shown as the figure 3.4 where kv and ks are voltage and current sensing gains, respectively. The following equation (3.11) can be acquired after combining sensing gain with the equation (3.10).

$$H_{dc}(s) = \frac{k_v k_{dc}}{k_s C s} \tag{3.11}$$

Figure 3.4

Voltage loop control block diagram



The voltage controller can be designed based on the loop gain from figure 3.4. Due to three phase rectifier DC voltage non-low frequency ripple, in order to lower down current command

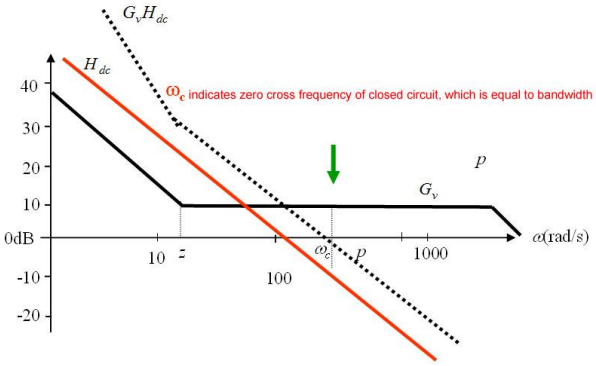
distortion, it doesn't need LPF (Low Pass Filter) to attenuate low frequency ripple of voltage 120Hz or 130Hz. Therefore, the controller utilizes PI (Proportional Integral) controller of which the transfer function is shown below:

$$G_v = \frac{k(s+z)}{s} \tag{3.12}$$

The frequency response between the equations (3.11) and (3.12) is illustrated as the figure 3.5 where ω_c indicates system zero cross frequency bandwidth and zero point select of G_v is supposed to make the zero cross frequency ω_c slope of $G_v H_{dc}$ as $-20db/decade$ under rated load. In light with the previous condition, it is able to design zero point and proportional gain constant k.

Figure 3.5

Voltage loop frequency response



Phase Lock Loop Design

The architecture of mentioned inverter phase lock loop is shown as the figure 3.6, which utilizes grid power voltage (Vsa, Vsb and Vsc) to acquire, after abc-αβ axis conversion, 2 signals Vmsin(ωt) and -Vmcos(ωt). The 2 signals multiply by the generated synchronous signals cos(ω1t) and sin(ω1t) to obtain the follows:

$$e = V_m\{\sin(\omega t)\cos(\omega_1 t) - \cos(\omega t)\sin(\omega_1 t)\} \tag{3.13}$$

According to the equation (3.13), if ω=ω1 and the equation (3.13) is equal to zero, phase lock loop controller can be designed based on this condition. The signal e, after a proportional integrator (PI),

acquires a frequency corrected signal Δω, which will be added into the original set frequency ωo(=314) to obtain a frequency ω1. The frequency ω1 will then, after integral, obtain an angle signal θ, which will, after 0~2π range limiter555555555333333333333333, check both Sine and Cosine tables to acquire cos(ω1t) and sin(ω1t) signals. The goal to achieve phase lock is realized through proportional integrator adjustion to further narrow down deviation e to zero; that is, ω=ω1.

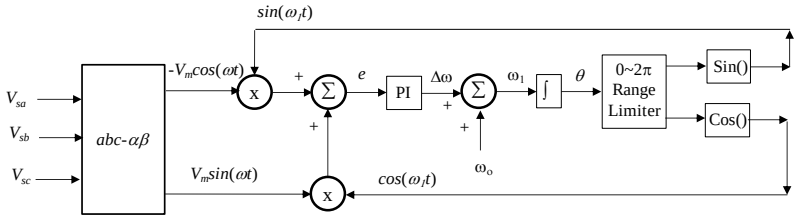


Figure 3.6 Phase lock loop

Circuit Simulation

The inverter specification

BUS Voltage V_{BUS} = 100V

AC Voltage V_{LL} = 50Vrms

Fs = 20kHz，Vtri = 10Vpp (PWM)

C_{BUS} = 940uF，L = 1.02mH，C = 10uF

Ks = 0.3 (AC current sensing factor)

Kv = 1/60 (AC voltage sensing factor)

Kv = 1/40 (DC voltage sensing factor)

The analogue circuit diagram based on the parameters above is as the following figure 3.7 shown:
PSIM File: PEK-550_Sim3_3P_GC_Inv(50Hz)_V11.1.5_V1.1

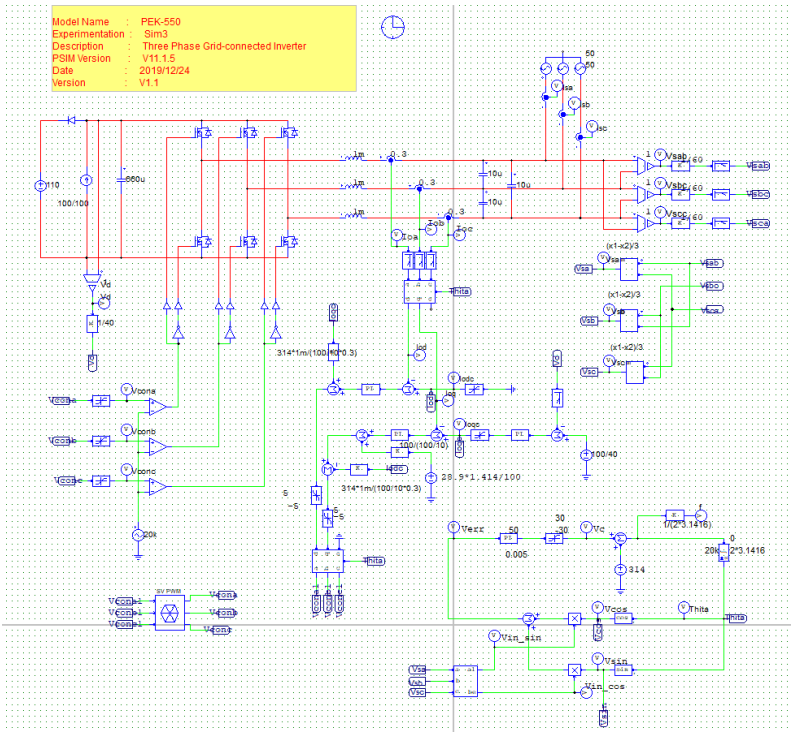


Figure 3.7 Experiment 3 PSIM analogue circuit diagram

The simulation result is shown within the figure 3.8 and 3.9:

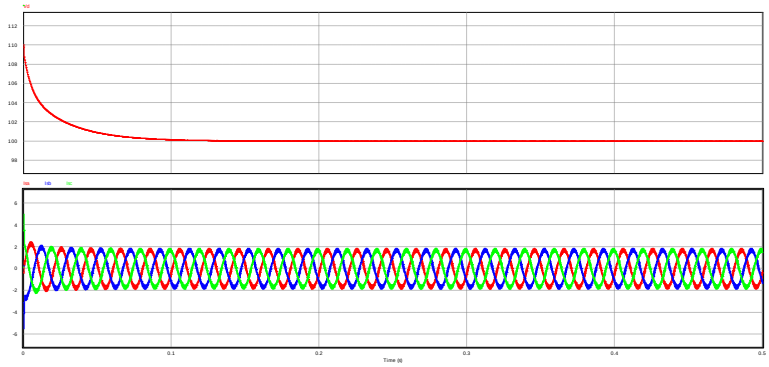


Figure 3.8 Experiment 3 analogue circuit simulation waveforms

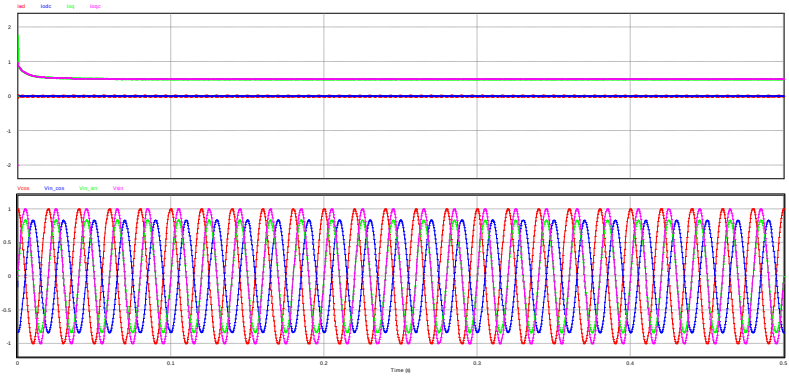


Figure 3.9 Experiment 3 analogue circuit simulation waveforms

The digital circuit diagram based on the analogue circuit is shown as the figure 3.10:
PSIM File: PEK-550_Lab3_3P_GC_Inv(50Hz)_V11.1.5_V1.1

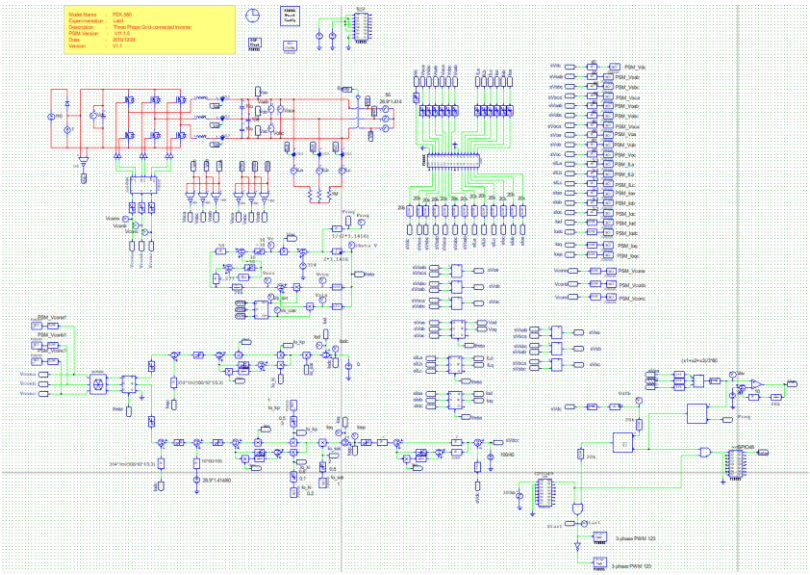


Figure 3.10 Experiment 3 PSIM digital circuit diagram

The simulation result is shown within the figure 3.11:

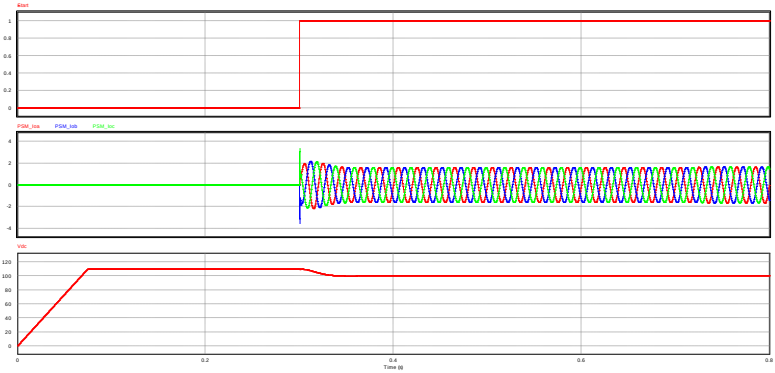


Figure 3.11 Experiment 3 digital circuit simulation waveforms

After confirming simulation, the corresponding C Code will be generated automatically via “Generate Code” of “Simulate”.

Experiment Devices

The required devices for experiment are as follows:

- PEK-550 * 1
- PEK-005A * 1
- PEK-006 * 1
- PTS-5000 * 1 (with GDS-2204E, APS-300, PSW160-7.2 and GPL-500)
- PC * 1

Experiment Procedure

1. The experiment wiring is shown as the figure 3.12. Please follow it to complete wiring.

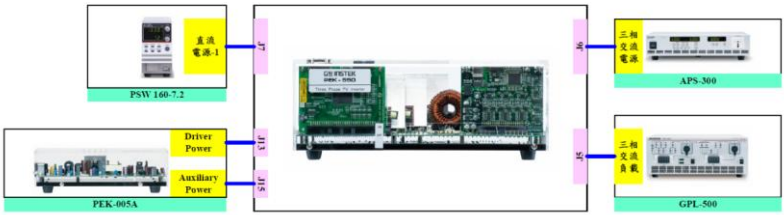


Figure 3.12 Experiment 3 wiring figure

2. After wiring, make sure the PEK-550 switch is OFF followed by turning the PEK-005A switch ON. The DSP red indicator lights on as the figure 3.13 shown, which means the DSP power is steadily normal.

Figure 3.13 DSP normal status with light on

3. Refer to the appendix B for burning procedure.
4. Connect the test leads of oscilloscope to Vo-AB, Vo-BC, Vo-CA and Io-A, respectively, as the figure 3.14 shown.

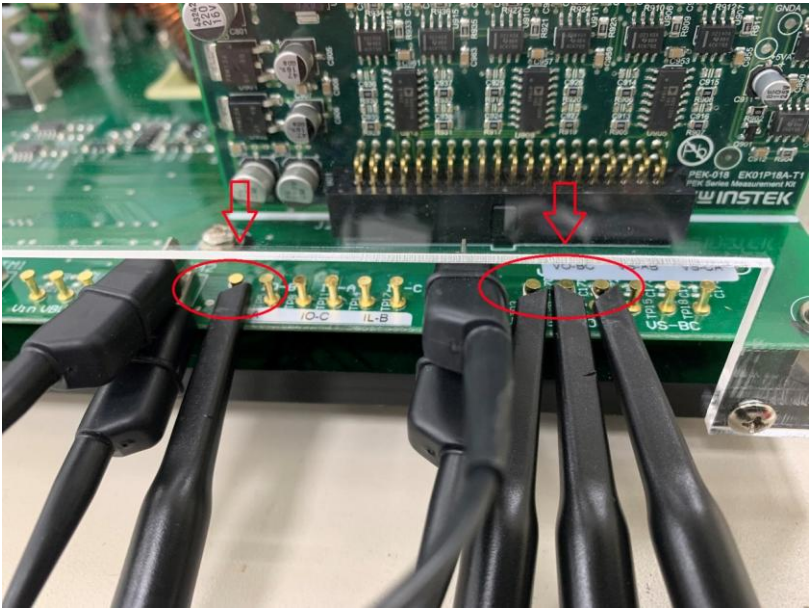


Figure 3.14 Oscilloscope test leads

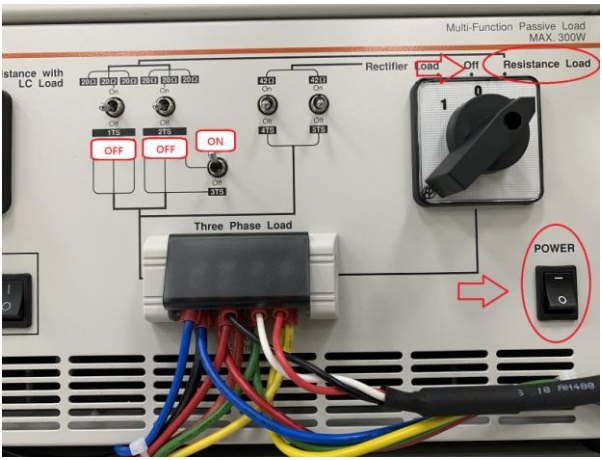
5. Set voltage 110V, current 1A for PSW160-7.2 as the figure 3.15 shown.

Figure 3.15 The settings of PSW-160-7.2

6. As the figure 3.16 shown, follow the steps below for GPL-500 operation. Power on GPL-500 → Rotate the Three Phase Lord knob to Resistance Load → Set 1TS and 2TS as OFF, and 3TS as ON, which indicates no-load mode.

Figure 3.16

The no-load setting of GPL-500



7. As the figure 3.17 shown, power on APS-300 and set 50Hz for frequency, 3P4W for mode, 28.86V for output voltage.

Figure 3.17

The setting of APS-300

8. After setting up, turn on PSW and APS-300 power output followed by powering on PEK-550.

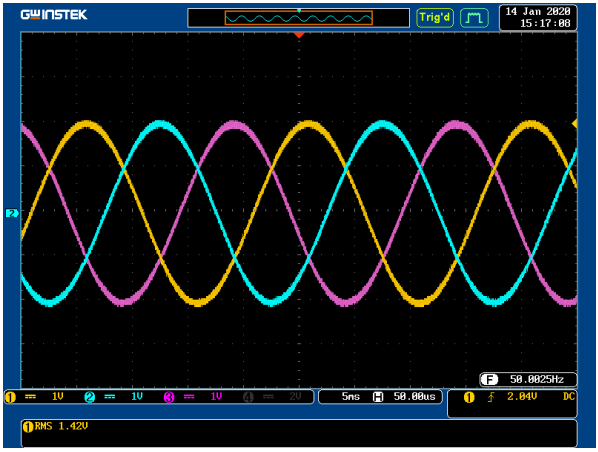
The experiment result

(5) No Load

The measured waveform of three phase voltage output Vo-AB, Vo-BC and Vo-CA is shown as the figure 3.18. Under the condition of no load, PSW output power is 100W. Due to without load, ASP-300 absorbs all the power and therefore it is seen that APS power is single phase -31.2W (negative sign indicates power absorbtion) and three phase total power is -31.2W*3= -93.6W, which is consistent with PSW output power (considering component loss) as the figure 3.19 shown.

Figure 3.18

The no-load measured waveforms



$V_{o_{ab}}$: $CH1(yellow)$: 1V/div $V_{o_{ca}}$: $CH3$(purple): 1V/div

$V_{o_{bc}}$: $CH2(blue)$: 1V/div

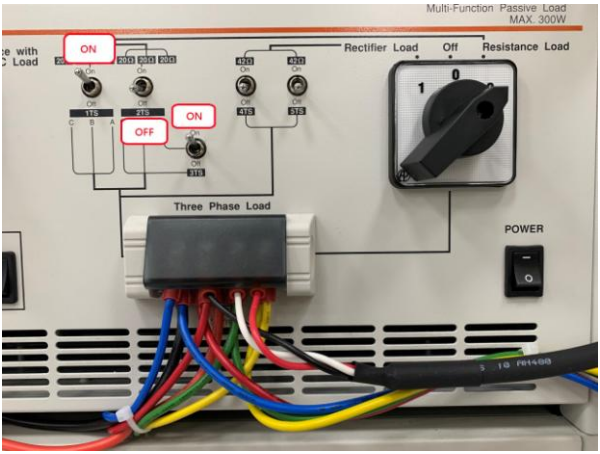
Figure 3.19 The power state of PSW and APS-300 when no load

(6) Half Load (20Ω)

Set 1TS and 3TS as ON, and 2TS as OFF as the figure 3.20 shown, which indicates hald load.

Figure 3.20

The half-load setting of GPL-500



Under the confition of half load, PSW output power is 100W and load is half load (125W). Because PSW output power can not meet requirement of load, APS-300 is supposed to providing 25W in order to maintain system power balance. It has seen that APS power is single phase 10.4W, and three phase total power is 10.4W*3 = 31.2W (considering component loss) as the figure 3.21 shown.

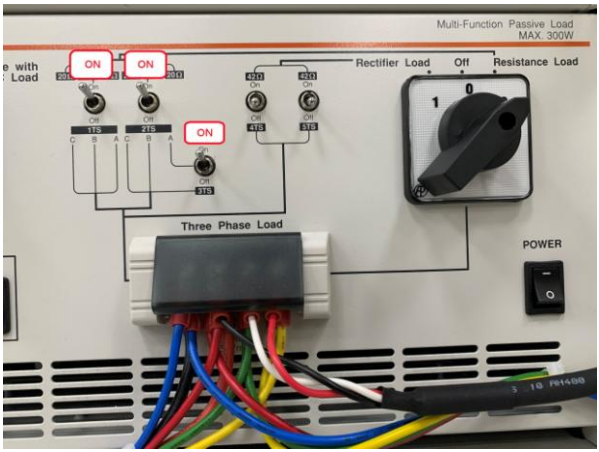
Figure 3.21 The power state of PSW and APS-300 when half load

(7) Full Load (10Ω)

Set 1TS, 2TS and 3TS as ON as the figure 3.22 shown, which indicates full load.

Figure 3.22

The full-load setting of GPL-500



Under the confition of full load, PSW output power is 100W and load is full load (250W). Because load requires larger power, APS-300 is supposed to providing 150W in order to maintain system power balance. It has seen that APS power is single phase 50.6W, and three phase total power is 50.6W*3 = 151.8W (considering component loss) as the figure 3.23 shown.

Figure 3.23 The power state of PSW and APS-300 when full load

After the experiment, power off PEK-550 followed by turning off PSW, APS-300 and GPL-500.

Fill in the table 3.1 with the power of PSW and APS-300 under varied load settings, individually.

Table 3.1 Power states of APS-300 in varied load settings.

	PSW Output Power	APS Output Power (considering component damage)	
No Load (0W)	100W	-93.6W	100 + (-93.6) ÷ 0
Half Load (125W)	100W	31.2W	100 + 31.2 ÷ 125
Full Load (250W)	100W	151.8W	100 + 151.8 ÷ 250

From the table 3.1, the power of power grid (simulating APS-300 in the experiment) either absorbs or provides power to maintain system power balance in accordance with varied load settings under the power grid system.

Experiment 4 – PV Boost Converter

Preview

1. Learn the characteristics of PV module
2. Learn the maximum power point tracking method of PV module
3. Learn the principle and design of double closed loop input voltage and current controller of boost converter
4. Learn PV array maximum power point tracking control of boost converter
5. Learn analog circuit establishment and simulation
6. Learn DSP digital control circuit plan

Experiment Content & Purpose

1. Use SAS software to control PSW and similate PV module manner
2. Use perturbation observation method to complete maximum power point tracking

Principle and Design

PV Module characteristics introduction

The output characteristic of PV module is neither constant voltage nor constant current. Because output power changes in light with working point, it is required to adjust working point dynamically in attempt to reach the best power generation, which is called MPPT (Maximum Power Point Tracking). The following describes more about the characteristic of PV module, which can be a reference for MPPT controller design.

PV module consists of several PV parallel series. After sunlight exposure, PV forms a current source which offers power for load. The PV equivalent circuit is shown as the figure 4.1 where Iph indicates current generated by PV, and Dj indicates a P-N junction diode, and Rsh with Rs indicate material internal resistors of equivalent in parallel and equivalent in series, respectively. In general, Rsh value is large, whilst Rs value is small when analysis. Therefore, in order to simplify analysis process, we discard values of Rsh and Rs. The Ip and Vp stand for PV output current and voltage, individually.

PV module equivalent circuit, P-N junction diode characteristic, and PV module output current can be expressed by the following mathametical equation (4.1):

$$I_{pv} = n_p I_{ph} - n_p I_{sat}\left[\exp\left(\frac{q}{kTA}\frac{V_{pv}}{n_s}\right) - 1\right] \qquad (4.1)$$

Vph: It indicates PV output voltage (V)

Ipv: It indicates PV output current (A)

T: It indicates PV surface temperature (°K)

A: It indicates PV ideal factor (A=1~5)

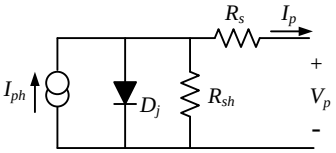
q: It indicates electric charge volume (1.6×10-19C)

k: It indicates Boltzmann constant (1.38×10-23 J/°K)

np: It indicates the number PV battery in parallel

ns: It indicates the number PV battery in series

Figure 4.1
PV equivalent circuit



Isat indicates PV panel inverse saturation current and the mathematical relation is shown below:

$$I_{sat} = I_{rr}(\frac{T}{T_r})^3 \cdot \exp[\frac{qE_{gap}}{kA}(\frac{1}{T_r} - \frac{1}{T})] \quad (4.2)$$

Tr: It indicates PV reference temperature (°K)

Irr: It indicates inverse saturation current when reference temperature is Tr (A)

Egap: It indicates the required power when semiconductor material crosses band gap

$$E_g = 1.16 - 7.02 \times 10^{-4} \frac{T^2}{T - 1108} \quad (4.3)$$

$$I_{ph} = [I_{scr} + \alpha(T - T_r)]\frac{S}{100}$$

Iscr: It indicates the short circuit current (A) when PV battery works in reference temperature and 1kW/m2 insolation exposure.

a: It indicates PV module short circuit current temperature coefficient

S: It indicates the insolation volume (kW/m2)

$$P_{pv} = V_{pv} \times I_{pv} \quad (4.4)$$

The following can be acquired by further substituting equation (4.1):

$$P_{pv} = n_p V_{pv} I_{ph} - n_p I_{sat} V_{ph}[\exp(\frac{q}{ktA}\frac{V_{pv}}{n_s}) - 1] \quad (4.5)$$

PV module characteristic can be realized via equation (4.5). It describes the PV module output voltage, current and power curve diagram under different insolation volume and PV panel surface temperature change.

The 75W PV module manufactured by Shell is shown as the table 4.1 below:

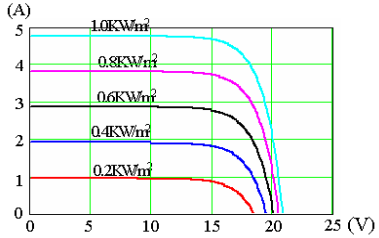
Table 4.1 Shell SQ85 PV specification

Electrical Characteristics	Spec
Rated Maximum Ouput Power (W)	75
Rated Current (A)	4.4
Rated Voltage (V)	17.0
Short Circuit Current Isc(A)	4.8
Open Circuit Voltage Voc(V)	21.7
Normal Working Temperature NOTC(°C)	45.2
Short Circuit Current Temperature Coefficient (mA/°C)	2.06
Open Circuit Voltage Temperature Coefficient (V/°C)	-0.77

Under the temperature of 25°C and sunlight insolation volume of 1KW/m2 from the table below, the electrical characteristics is shown as the table 4.1. Under different insolation volume, the curve of output voltage to current and the curve of output voltage to power are shown as the figure 4.2(a) and 4.2(b), respectively. And under different temperature, the curve of output voltage to current and the curve of output voltage to power are shown as the figure 4.3(a) and 4.3(b), respectively.

Figure .42

(a) The characteristics curve of Ip-Vp under different insolation and fixed environmental temperature (25°C)



(b) The characteristics curve of P-Vp

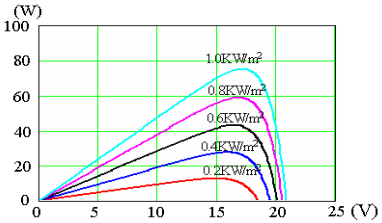
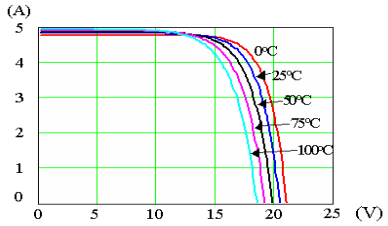
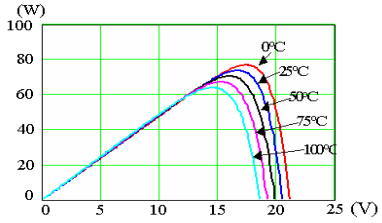


Figure 4.3

(a) The characteristics curve of Ip-Vp under different environmental temperature and fixed insolation (1kW/m²)



(b) The characteristics curve of P-Vp



PV Converter Control Method

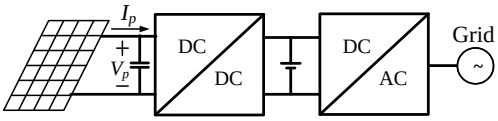
From the characteristics simulating curve of PV module, we can understand that the 2 factors influencing PV module output power

are insolation intensity and environmental temperature. In light with fluctuations of weather, both temperature and insolation intensity will change accordingly. Hence, in order to have the maximum output power and enhance generation efficiency of PV module, it is required to control power converter of PV system to reach the maximum power output under differenct working environments, which is the so-called MPPT (Maximum Power Point Tracking).

The figure 4.4 indicates grid power in parallel system where MPPT control can be achieved by controlling input voltage Vp and input current Ip of PV module converter to calculate the voltage of maximum power point of PV module, which will be regarded as command, and to operate exactly on MPPT point via voltage loop control.

Figure 4.4

Two-stage grid power in parallel system

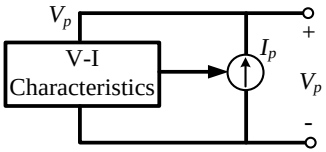


From the characteristics simulating curve of PV module, we can understand that PV module is neither voltage source nor current source. When applying to synthesized analysis of voltage source converter as the figure 4.4 shown, PV module must be regarded as a current source, and the equivalent circuit is shown as the figure 4.5(a). In contrast, when applying to current source converter, PV module must be regarded as a voltage source, and the equivalent circuit is shown as the figure 4.5 (b).

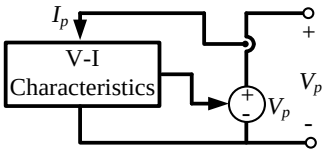
Figure 4.5

PV module equivalent circuit

(a) Voltage source converter



(b) Current source converter



MPPT Method

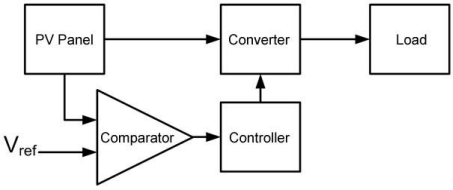
In terms of MPPT method, there have been several methods available including voltage feedback, power feedback, perturbation and observation, incremental conductance, linear approximation and practical measurement, all of which belong to maximum power tracking method and share the identically common concept. They utilize PV output voltage or current or both to realize the maximum power tracking method. The main difference is the diversity of judgement and realization of maximum power point. Refer to the follows for the MPPT control methods:

(9) Voltage Feedback

As the figure 4.6 shown, the voltage feedback is the simplest method which reaches the purpose of maximum power tracking, via adjusting PV module output voltage, under the known insolation intensity and temperature. The main deficiency is that when temperature changes, the system is not able to track the latest maximum power point and further causes power loss.

Figure 4.6

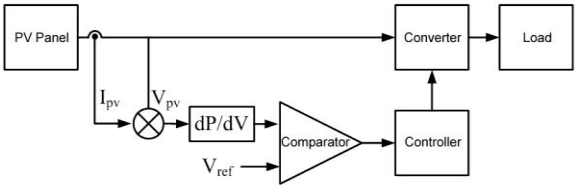
Voltage feedback block diagram



(10) Power Feedback

As the figure 4.7 shown, power feedback is almost identical with voltage feedback. Because voltage feedback is not able to track the latest power point under the condition of fluctuating atmosphere, the judgement of rate of change of output power to voltage is added into power feedback in order to track the maximum power point when facing atmospheric condition change. Though the additional voltage fluctuation rate of change judgement is added into voltage feedback, power loss is reduced instead and the efficiency is much better than voltage feedback.

Figure 4.7
Power feedback block diagram



(11) Perturbation Observation

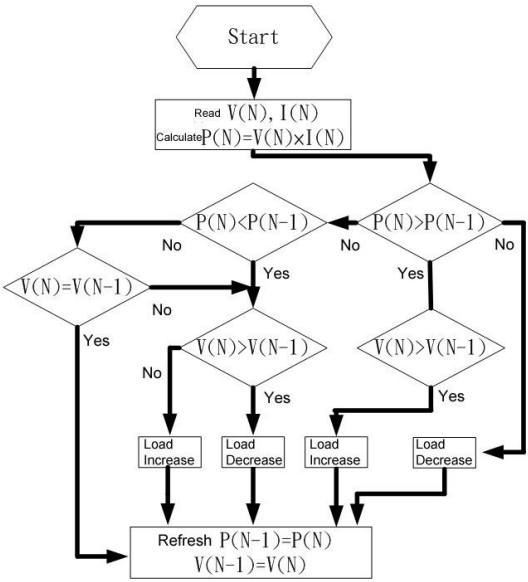
As the figure 4.8 shown, perturbation observation, which is simple in terms of structure, only measures PV module output voltage and current as thus, similar to power feedback, can be generally applied to PV module maximum power tracking.

The basic principle of perturbation observation is to change PV module output voltage and current via scale of load of cyclic increase or decrease. That is, to change working point from characteristics curve of PV panel and observe with comparing output voltage and output power scale before/after load fluctuation followed by determining next move of increase or decrease load.

If perturbation results in PV module output power increase compared with the previous time, increase or decrease load properly for same direction in the next cycle in order to increase output power continuously. In contrast, if output power is less than that before fluctuation, it is required to change load fluctuation direction in the next cycle. By repeating perturbation and observation, PV module can reach the maximum power point, which is the very principle of Perturbation Observation. If response

speed is fast enough, voltage fluctuation intensifies. Therefore, it has to make a trade-off between accuracy and response speed.

Figure 4.8 Perturbation Observation block diagram



(12) Increamental Conductance, INC

As the figure 4.9 shown, the concept of increamental conductance is identical to power feedback, mainly utilizing judgement, which can be rephrased as follows:

$$\frac{dP_{pv}}{dV_{pv}} = \frac{d(I_{pv}V_{pv})}{dV} = I + V\frac{dI}{dV} = 0 \tag{4.9}$$

The following can be acquired by arranging the equation (4.9):

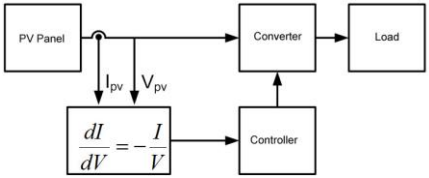
$$\frac{dI}{dV} = -\frac{I}{V} \tag{4.10}$$

From the equation (4.10), dI indicates the measured current variation before/after incremental, whilst dV indicates the measured voltage variation before/after incremental. The next time variation can be determined via measuring incremental value dI/dV and PV conductance I/V. When incremental value and conductance fit the relation of equal on both sides, it signals the maximum power point has been reached and thus next

perturbation will not be processed, which is the basic theory of incremental conductance.

Although incremental conductance reaches the maximum power tracking to meet the maximum power point by changing PV module output voltage, the issue of oscillation, different from the judgement logic of perturbation observation, in the proximity of maximum power tracking, which usually occurs in perturbation observation, can be effectively avoided.

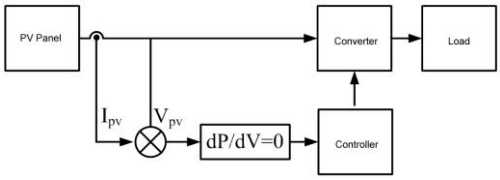
Figure 4.9
Incremental conductance block diagram



(13) Linear Approximation

As the figure 4.10 shown, the basic concept of linear approximation employs the logical judgement of $dP_{pv}/dV = 0$ and utilizes a linear line to approximate the maximum power point of PV module under fixed temperature with varied insolation volume. Further, it controls PV module output current within the linear line to reach the maximum power tracking. We figure out the approximate linear line on the maximum power point of PV module in light with basis of mathematical model where accuracy of each factor along with component aging will affect accuracy of linear approximation by certain margin.

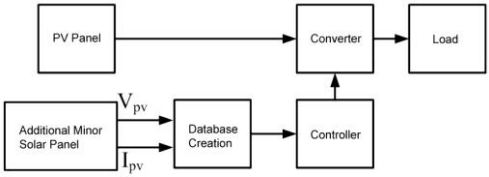
Figure 4.10
Linear approximation block diagram



(14) Pratical Measurement

As the figure 4.11 shown, practical measurement mainly takes advantage of additional PV module to measure open-circuit voltage and short-circuit current of PV panel at intervals. The voltage and current of maximum power point under the insolation and temperature in the established atmospheric condition make PV module work and gain the precisely maximum power point in association with control circuit. However, this condition only applies to the region with fair climate change. If condition changes, it requires remeasurement for database establishment, which is the main defect.

Figure 4.11 Pratical measurement block diagram



The comparison table of pros and cons and working principle of maximum power tracking is shown as the table 4.2.

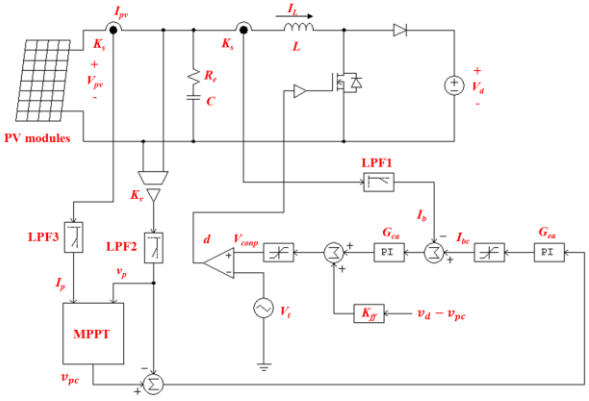
Table 4.2 Comparison table of pros and cons and working principle of maximum power tracking

MPPT Method	Working Principle	Pros	Cons
Voltage Feedback	Refer to the PV board characteristics by prior measurement	Simple architecture with low cost	Not available for auto tracking the latest maximum power point
Power Feedback	Indentical to the voltage feedback, it increases power output to judge voltage change	Lessen energy consumption whilst increase the overall efficiency	Identical to the voltage feedback, it has larger calculation amounts
Perturbation Observation	Increase load in cycle and observe power and voltage changes to determine load	Easy implement with simple architecture	Fluctuating power loss occurs on the maximum power

	increase or decrease in next the step	and principle	point
Incremental Conductance	Utilize the relation between PV dI/dV and I/V to determine incremental value	It lessens fluctuating power loss compared with pertube and observe method	It requests highly precise accuracy for measurement with wider errors in actual application
Linear Approximation	Via dP/dV=0, it utilizes a linear to similize PV maximum power point	Easy implement with simple architecture	Accuracy deteriorates when PV board and components have aged
Practical Measurement	Externally connect to a PC board to measure characteristics and establish reference model for control	Prevent PV from aging that deteriorates the accuracy of model	It requires remeasurement to establish database when environment changes

This experiment utilizes perturbation observation to complete MPPT control. The circuit control architecture is shown as the figure 4.12.

Figure 4.12 Control architecture



The following can be acquired via the figure 4.12 with the state average:

$$L_b \frac{dI_b}{dt} = V_b - (1-d)V_d \tag{4.11}$$

The Duty can be expressed as follows:

$$d = \frac{v_{con}}{V_{tm}} \tag{4.12}$$

The following can be obtained via substitute:

$$L_b \frac{dI_b}{dt} = V_b - (1 - \frac{v_{con}}{V_{tm}})V_d \tag{4.13}$$

The following equation can be acquired by arrangement:

$$L_b \frac{dI_b}{dt} = \frac{V_d}{V_{tm}} v_{con} + V_b - V_d \tag{4.14}$$

Further substitute $k_{pwmb} = \frac{V_d}{V_{tm}}$

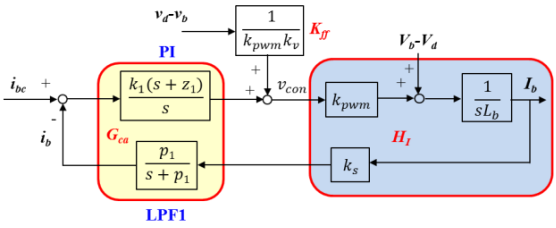
$$L_b \frac{dI_b}{dt} = k_{pwmb}\, v_{con} + V_b - V_d \tag{4.15}$$

The equation (4.15) is used to design current controller of boost converter.

Cuccrent Controller Design

The current loop control block based on the equation (4.15) is shown as the figure 4.13 where Ks and Kv are voltage and current sensing gain, respectively, which utilize feedback control along with feedforward control to compensate the perturbation from Vb-Vd to current loop.

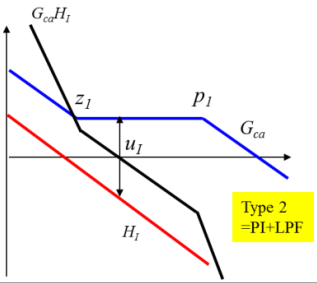
Figure 4.13
Current loop control block diagram



The current controller of this circuit is the second-class deviation amplifier, which can be separated into a proportional integral controller (PI) and a low pass filter (LPF). The bode plot along with design methid is shown as the figure 4.14 below.

Fogire 4.14

Current loop frequency response bode plot



1. Set u_I as 1/10 ~ 1/8 of switch frequency
2. Set $z = \frac{u_I}{3}$ $Z = \frac{u_I}{3}$
3. Set $p = \frac{f_s}{2}$ (low pass filter)
4. Set $G_{ca}(u_I)H_I(u_I) = 1$ for k_1

Voltage Controller Design

General the response speed of voltage loop is far lower than that of current loop. Hence, when modeling voltage loop, it is available to regard current loop as ideal. That is, sensing conductance current and command response should be regarded as 1, on the basis of which, voltage loop equivalent circuit can be simplified as the figure 4.15. And the following can be acquired from the figure 4.15:

$$\frac{V_p}{I_L} = -\frac{1+\frac{s}{\omega_z}}{sC}, \quad \omega_z = \frac{1}{CR_e} \tag{4.16}$$

The voltage loop control block diagram, which is drawn based on the equation (4.16), is shown as the figure 4.16 where voltage deviation amplifier (Gea) can be designed by the previous second-class deviation amplifier as the figure 4.17 shown in which voltage

loop bandwidth can be designed at the 1/3 ~ 1/5 of current loop bandwidth.

Figure 4.15
Voltage loop equivalent circuit

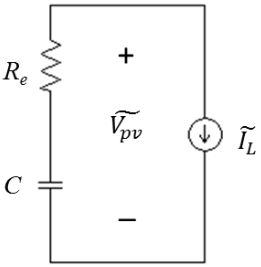


Figure 4.16
Current loop control block diagram

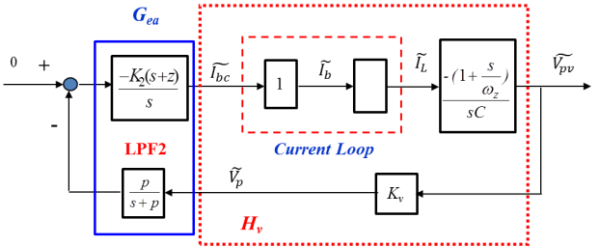
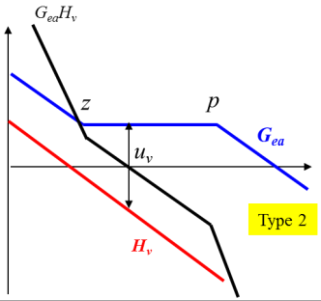


Figure 4.17
Voltage loop frequency response bode plot



The control loop parameters are designed by Matlab. The program is shown as follows:

```
% Boost Input Voltage Control
clf;
clc;
PI = 3.1416;
Vpv = 70;
Vd = 100;
Pi = 150;
L = 660e-6;
C = 200e-6;
Re = 0.03;
fs = 40e3;
ws = 2* PI * fs;
Ts = 1/fs;
Vtm = 5;
Kv = 1/40;
Ks = 0.6;
% PWM
D = 1 - Vpv/Vd;
Vcon = D * Vtm;
% Small signal model of current loop
Kpwm = Vd/Vtm;
numHi = Ks * Kpwm/L;
denHi = [1 0];
Hi = tf(numHi, denHi);
```

```
% Current controller Type2 Gca(s)=
K1(s+z)/s * p/(s+p)
ui = ws/10;
fcoi = ui/(2*PI)
Hr = freqresp(Hi, ui);
GainH = abs(Hr);
GainGca = 1/GainH;
zi = ui/3;
tui = 1/zi
numG1 = [1 zi];
denG1 = [1 0];
G1 = tf(numG1, denG1);
pi = 2 * PI * 10e4
numLPF1 = pi;
denLPF1 = [1 pi];
LPF1 = tf(numLPF1, denLPF1);
G1f = G1 * LPF1;
G1r =  freqresp(G1f, ui);
K1 = GainGca/abs(G1r)
Gca = K1 * G1f;
GcaHi = series(Gca, Hi);
GcaHr =  freqresp(GcaHi, ui);
phaseGcaHr = angle(GcaHr) * 180/PI;
PMi = 180 + phaseGcaHr
figure(1);
bode(Hi, Gca, GcaHi);
grid;
```

```
% Small signal model of voltage loop
wz = 1/(Re * C);
numHv = Kv/(Ks * C) * [1/wz  1];
denHv = [1 0];
Hv = tf(numHv, denHv);
% Voltage controller Type2 Gea(s)= K2(s+z)/s * p/(s+p)
uv = ui/8;
fcov = uv/(2*PI)
Hvr = freqresp(Hv, uv);
GainHv = abs(Hvr);
GainGea = 1/GainHv;
zv = uv/3;
tuv = 1/zv
numG2 = [1 zv];
denG2 = [1 0];
G2 = tf(numG2, denG2);
pv = 2 * PI * 10e4
numLPF2 = pv;
denLPF2 = [1 pv];
LPF2 = tf(numLPF2, denLPF2);
G2f = G2 * LPF2;
G2r =  freqresp(G2f, uv);
K2 = GainGea/abs(G2r)
Gea = K2 * G2f;
GeaHv = series(Gea, Hv);
GeaHvr =  freqresp(GeaHv, uv);
phaseGeaHvr = angle(GeaHvr) * 180/PI;
PMv = 180 + phaseGeaHvr
figure(2);
bode(Hv, Gea, GeaHv);
grid;
```

The result is as follows:

fcoi = 4000 (Hz) (bandwidth of current loop)
tui = 1.1937e-04 (time constant of current PI controller)
pi = 628320 (LPF1 pole)
K1 = 1.6405 (gain of current PI controller)
PMi = 69.2747 (phase margin of current control loop)
fcov = 500 (Hz) (bandwidth of voltage loop)
tuv = 9.5493e-04 (time constant of voltage PI controller)
pv = 628320 (LPF2 pole)
K2 = 14.3035 (gain of voltage PI controller)
PMv = 72.3587 (phase margin of voltage control loop)

The MPPT program based on P&O method is shown below:

```
static int n;
static double ymax = 50;
static double ymin = 24;
static double Vp, Ip, Vp1, Ip1, P, P1, dP, dv=1, Vpc, Vpc1, start, CLK,
CLK1;
start = x3;
Vp = x1;
Ip = x2;
CLK = x4;
P = Vp * Ip;
if (start <1)
{
Vpc = Vp - dv;
CLK1 = CLK;
}
if (start >0)
{
    if((CLK-CLK1)==1)
  {
      if (P > P1)
    {
       if (Vp > Vp1)
          { Vpc = Vp + dv; }
       else
          { Vpc = Vp - dv;  }
     }
  else
     {
       if (Vp > Vp1)
```

```
            { Vpc = Vp - dv; }
          else
            { Vpc = Vp + dv;  }
        }
   if (Vpc>=ymax)
    { Vpc= Vp - dv;}
   if (Vpc<=ymin)
    { Vpc= Vp + 3 * dv;}
    Vp1 = Vp;
    Vpc1 = Vpc;
    dP = P - P1;
    P1 = P;
     }
  CLK1 = CLK;
 }
y1=Vpc;
y2 = P;
y3 = dP;
```

Circuit Simulation

Boost converter specification is as follows:

DC Input Voltage V_b = 70V

DC bus Voltage Vd = 100V

Fs = 40kHz，V_{tri} = 5V_{PP} (PWM)

C_b = 200uF，L_b = 660uH

Ks = 0.6 (DC current sensing factor)

Kv = 1/40 (DC voltage sensing factor)

The analogue circuit diagram based on the parameters above is as the following figure 4.18 shown:
PSIM File: PEK-550_Sim4_PV_Boost_V11.1.5_V1.1

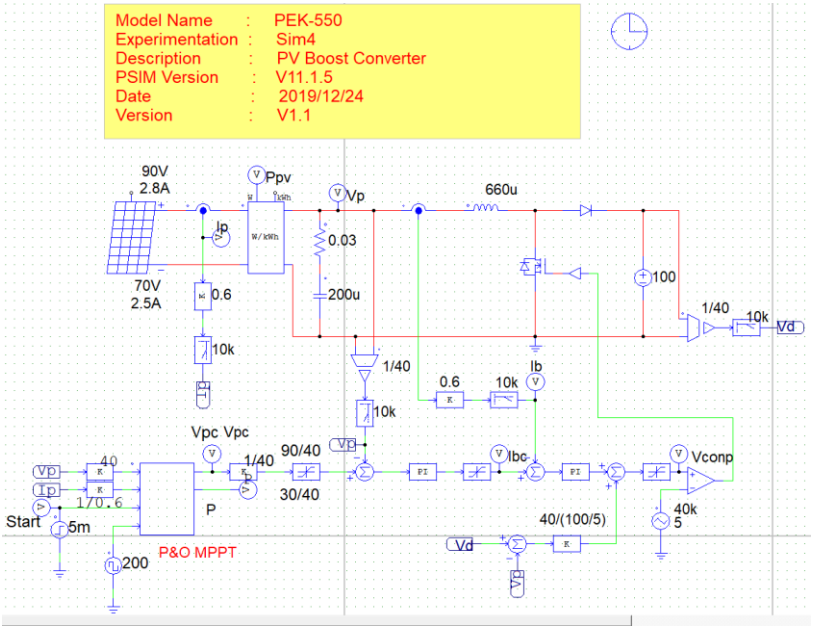


Figure 4.18 Experiment 4 PSIM analogue circuit diagram

The simulation result is shown within the figure 4.19:

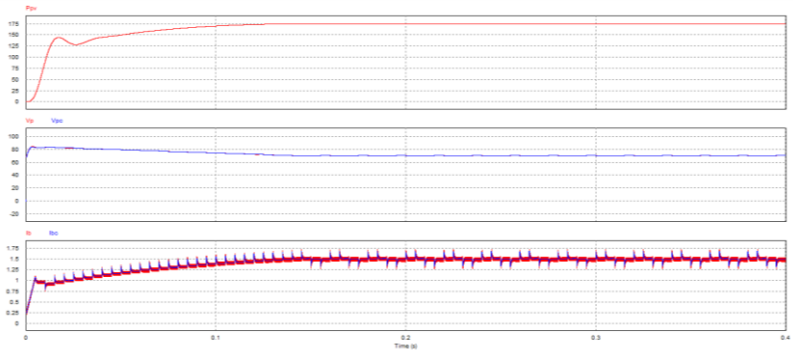


Figure 4.19 Experiment 4 analogue circuit simulation waveforms

The digital circuit diagram based on the analogue circuit is shown as the figure 4.20:
PSIM File: PEK-550_Lab4_PV_Boost_V11.1.5_V1.1

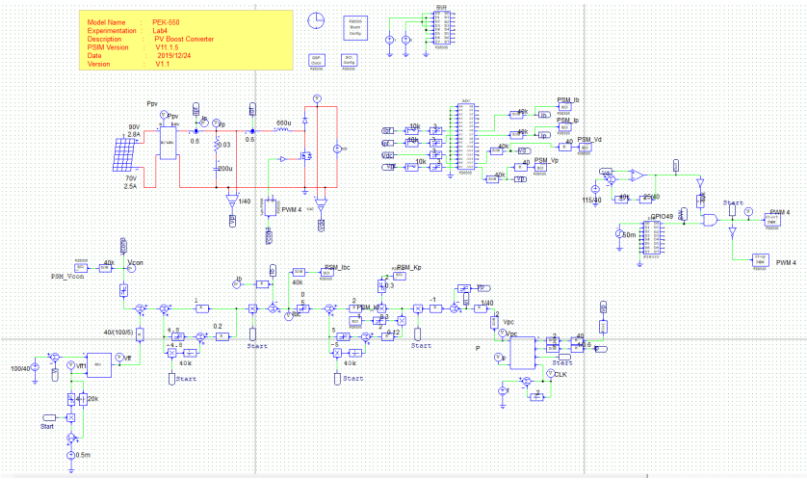


Figure 4.20 Experiment 4 PSIM digital circuit diagram

Because the circuit, which practically generates Code, has the MPPT adjusted frequency 2Hz and it is time-consuming for simulation based on this circuit file, we alternately provide another

digital circuit, “PEK-550_Sim4D_PV_Boost_V11.1.5_V1.1”, of MPPT adjusted frequency 100Hz, based on which it requires relatively shorter period for simulation result. Refer to the figure 4.21 for the simulation result.

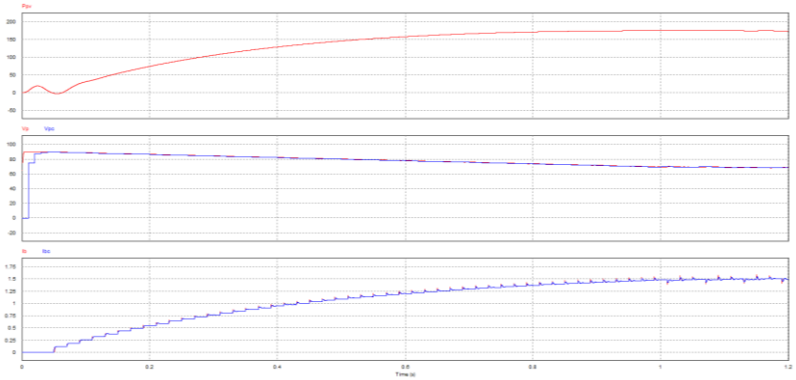


Figure 4.21 Experiment 4 digital circuit simulation waveforms

After confirming simulation, the corresponding C Code will be generated automatically via “Generate Code” of “Simulate”.

Experiment Devices

The required devices for experiment are as follows:

- PEK-550 * 1
- PEK-005A * 1
- PEK-006 * 1
- PTS-5000 * 1 (with PSW160-7.2 and PEL-3031E)
- PC * 1

Experiment Procedure

1. The experiment wiring is shown as the figure 4.22. Please follow it to complete wiring.

Figure 4.22 Experiment 4 wiring figure

2. After wiring, make sure the PEK-550 switch is OFF followed by turning the PEK-005A switch ON. The DSP red indicator lights on as the figure 4.23 shown, which means the DSP power is steadily normal.

Figure 4.23 DSP normal status with light on

3. Refer to the appendix B for burning procedure.
4. Refer to the appendix D – SAS software operation manual for PV system setting process in simulation. As the figure 4.24 shown, the open circuit voltage of first curve is 90V, and the short circuit current is 2.8A with the MPP voltage 70V along with the MPP current 2.5A. As the figure 4.25 shown, the value of second curve is set 90% of the first MPP. The open circuit voltage of the second MPP, therefore, is 81V, and the short circuit current is 2.52A with the MPP voltage 63V along with the MPP current 2.25A.

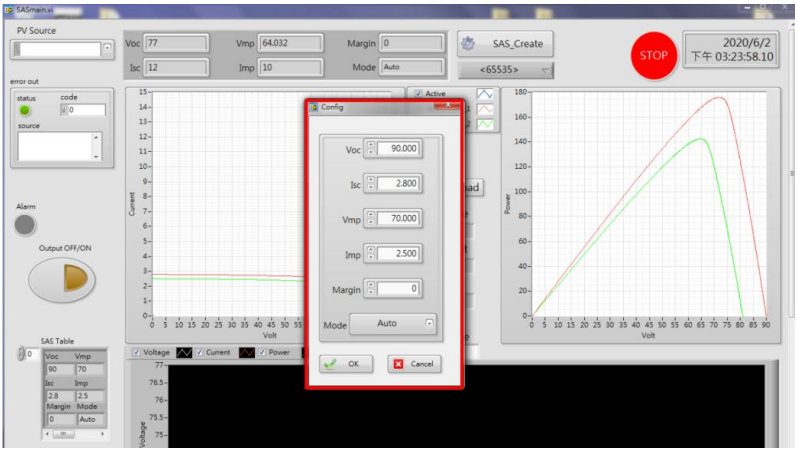


Figure 4.24 The 1st curve setting value

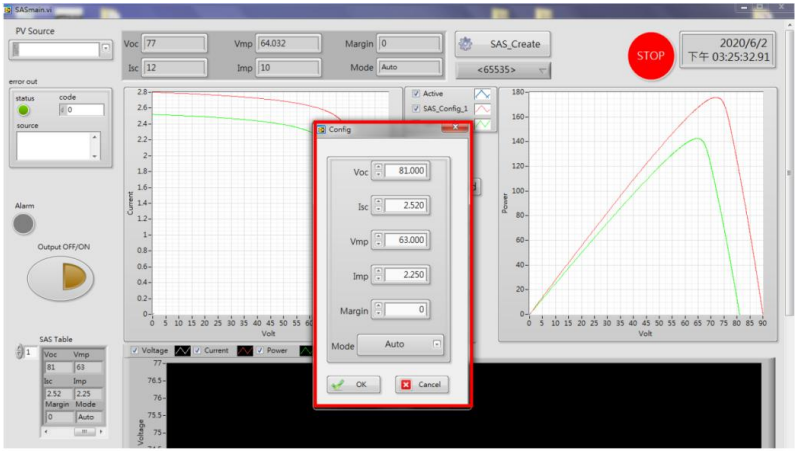


Figure 4.25 The 2nd curve setting value

5. After powering on PEL-3031E, set voltage 100V in CV mode and activate load function as the figure 4.26 shown.

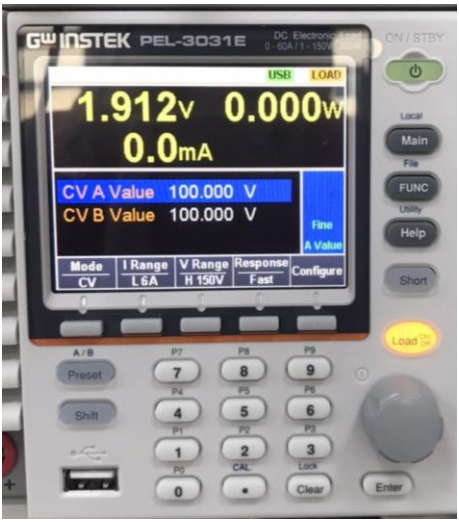


Figure 4.26 PEL-3031E operates under CV mode

6. After setting, launch PSW power output followed by powering on PEK-550.

The experiment result

This experiment, which simulates that PV panel receives intensifying lights and is impacted by environmental factors, outputs power fluctuately. In order to fully manipulate, it makes operation fixed in the MPP via the MPPT method. From the SAS program, it has seen that output power of I-V and P-V curves approaches the maximum power point gradually as the figure 4.27 and 4.28 shown.

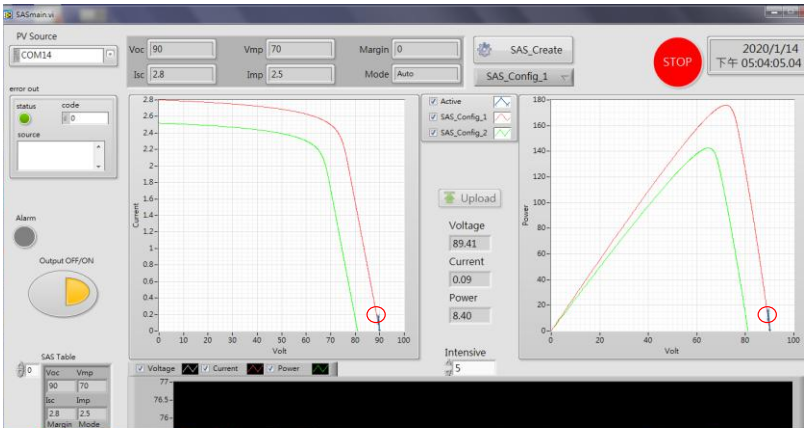


Figure 4.27 SAS initial startup state

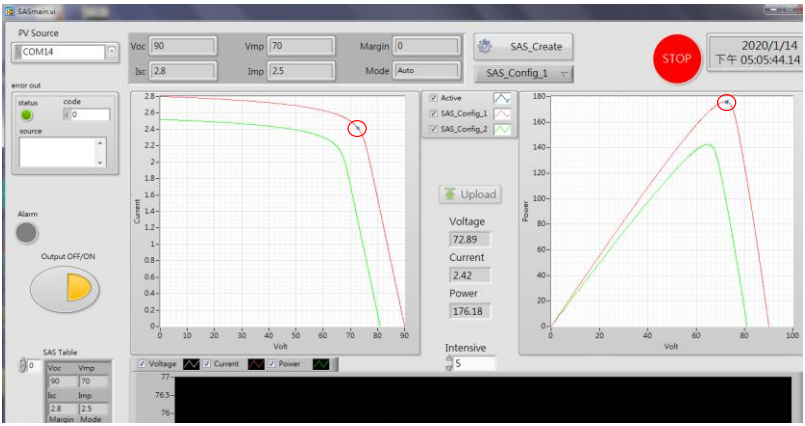


Figure 4.28 SAS exists in the maximum power point of the 1st curve

I-V and P-V curves are subject to influences from environmental factors and thus result in varied curves. As the figure 4.29 shown, when curve changes to I-V and P-V curves, the output power is maintained still and is approaching the maximum power point gradually. See the figure 4.30 shown.

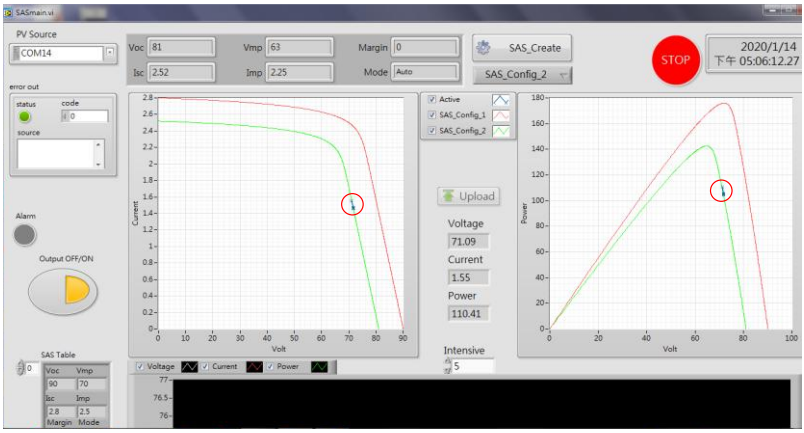


Figure 4.29 SAS changes vaired PV curves

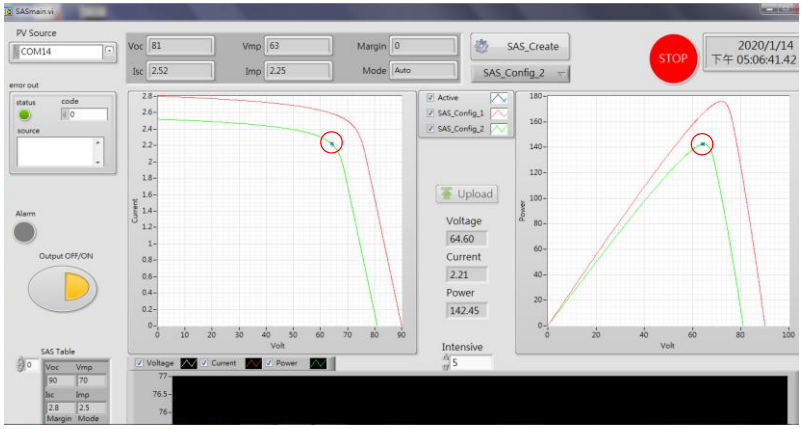


Figure 4.30 SAS exists in the maximum power point of the 2nd curve

It has seen that, from the above results, MPPT control function of PEK-550 is able to maintain the maximum power output for PV panel. Though PV curve varies due to environmental factor, the highest utilization rate can be reached still.

Experiment 5 – Three Phase Islanding Protection Inverter

Preview

1. Understand the voltage and frequency specification of distributed power
2. Learn voltage and frequency calculation
3. Learn active and passive islanding effect detection
4. Learn design of sliding mode frequency offset islanding effect detection
5. Learn simulating circuit establishment and simulation
6. Learn DSP digital control circuit plan
7. Validate voltage and frequency protection as well as islanding effect protection

Experiment Contents and Purpose

1. Build grid-connected system under islanding effect after power grid is removed
2. Make inverter escape under islanding effect via AFD method

Principle and Design

When PV inverter is grid-connected, it works normally based on power grid voltage. After power grid voltage is removed, inverter stops operation logically. If inverter keeps operation, we call it "islanding effect" in which the harmonic frequency formed by conductance and capacitor of whole system is in proximity of the power grid frequency. Hence, inverter is not able to detect that power grid has been removed, and anti-islanding effect mechanism is necessary to add into inverter system so that inverter can escape successfully even under this condition. We list several specifications relevant to islanding effect as the table 5.1 and 5.2 below, from which we may understand that escaping time specifications vary per different voltage and frequency ranges.

Table 5.1 Voltage specification

Item / Standard	Voltage Range (% standard voltage)	Escape Time (second)
IEEE Std. 1547	V<50	0.16
	50≤V<88	2.00
	88≤V≤110	Normal
	110<V<120	1.00
	120≤V	0.16
UL 1741	V<50	0.1
	50≤V<88	2.00
	88≤V≤110	Normal
	110<V<120	2.0
	137≤V	0.033

Table 5.2 Frequency specification

Item / Standard	Frequency Range		Escape Time (second)
IEEE Std. 1547	≤30kW	> 60.5	0.16
		< 59.3	0.16

	>30kW	> 60.5	0.16
		<{59.8~57.0}	0.16~300
		< 57.0	0.16
UL 1741	f > 60.5		0.1
	59.3≤ f ≤60.5		Normal
	f ≤59.3		0.1

As the figure 5.1 shown, islanding effect detection is divided into 2 tpyes: active and passive. The figure 5.3 illustrates the most common detection method. When turning on the switch, passive detection takes advantage of ΔP and ΔQ, which are non-zero hour voltage and frequency changes, to know grid power outage. However it comes with larger non-detection zone (NDZ) instead.

Figure 5.1
Islanding effect test illustration

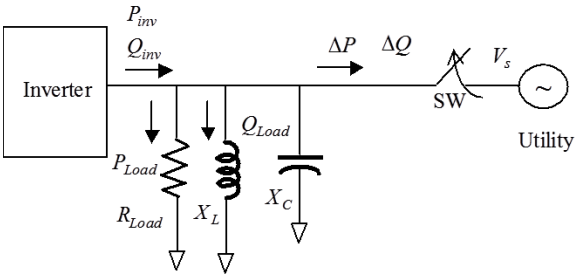


Table 5.3 Islanding detection method

Passive	1. Over/under Voltage 2. Over/under Frequency 3. Voltage Phase Jump 4. Detection of Voltage Harmonics 5. Detection of Current Harmonics
Active	1. Impedance Measurement 2. Detection of Impedance at a Specific Frequency 3. Slip-mode Frequency Shift (SMS) 4. Frequency Bias 5. Active FrequencyDrift (AFD) 6. Voltage Shift 7. Frequency Jump

The following discusses the existed NDZ area of passive islanding detection. And the equation below is created by the power condition of grid power in parallel as the figure 5.1 shown.

$$\Delta P = P_{inv} - P_{Load} \tag{5.1}$$

$$\Delta Q = Q_{inv} - Q_{Load} \tag{5.2}$$

$$P_{Load} = \frac{V_s^2}{R} \tag{5.3}$$

$$Q_{Load} = V_s^2\left(\frac{1}{\omega L} - \omega C\right) \tag{5.4}$$

$$\omega_R = \frac{1}{\sqrt{LC}} \tag{5.5}$$

$$Q_f = R\sqrt{\frac{C}{L}} \tag{5.6}$$

The equation (5.7) is acquired via arrangement of equation (5.3).

$$R = \frac{V_s^2}{P_{Load}} \tag{5.7}$$

The following equation can be acquired via substituting equation (5.7) into (5.4):

$$Q_{Load} = V_s^2\left(\frac{1}{\omega L} - \omega C\right) = P_{Load}\, R Q_f \frac{1}{Q_f}\left(\frac{1}{\omega L} - \omega C\right)$$

$$Q_{Load} = V_s^2\left(\frac{1}{\omega L} - \omega C\right) = P_{Load} R Q_f \frac{1}{Q_f}\left(\frac{1}{\omega L} - \omega C\right) \tag{5.8}$$

Further substitute and arrange equation (5.6):

$$Q_{Load} = P_{Load}\, Q_f \frac{R}{R\sqrt{\frac{C}{L}}}\left(\frac{1}{\omega L} - \omega C\right) = P_{Load}\, Q_f\left(\frac{1}{\omega\sqrt{LC}} - \omega\sqrt{LC}\right)$$

$$Q_{Load} = V_s^2\left(\frac{1}{\omega L} - \omega C\right) = P_{Load} R Q_f \frac{1}{Q_f}\left(\frac{1}{\omega L} - \omega C\right) \tag{5.9}$$

$$Q_{Load} = P_{Load}\, Q_f\left(\frac{\omega_o}{\omega} - \frac{\omega}{\omega_o}\right) = P_{Load}\, Q_f\left(\frac{f_o}{f} - \frac{f}{f_o}\right)$$

$$Q_{Load} = V_s^2\left(\frac{1}{\omega L} - \omega C\right) = P_{Load} R Q_f \frac{1}{Q_f}\left(\frac{1}{\omega L} - \omega C\right) \tag{5.10}$$

Via equation (5.1) it can be written as follows:

$$P_{inv} = P_{Load} - \Delta P = V_s I_o \tag{5.11}$$

$$I_o = \frac{P_{Load} - \Delta P}{V_s} \tag{5.12}$$

When grid power escapes, the equation can be expressed as follows where V_a indicates PCC point end voltage after escape.

$$V_a = I_o R \tag{5.13}$$

Further substitute equation (5.7) and (5.10) for arrangmenet.

$$V_a = I_o R = \frac{P_{Load} - \Delta P}{V_s} \cdot \frac{V_s^2}{P_{Load}} = V_s(\frac{P_{Load} - \Delta P}{P_{Load}}) \tag{5.14}$$

$$V_a = V_s(1 - \frac{\Delta P}{P_{Load}}) \tag{5.15}$$

$$\frac{\Delta P}{P_{Load}} = 1 - \frac{V_a}{V_s} \tag{5.16}$$

We presume that voltage range is gri-connected normal range as the equation (5.15) shown.

$$V_{s,min} \leq V_a \leq V_{s,max} \tag{5.17}$$

Substitute equation (5.15) into (5.14) and the NDZ area of real power can be obtained as the equation (5.18) shown.

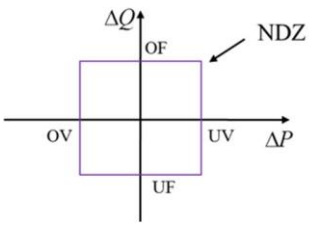
$$1 - \frac{V_{s,max}}{V_s} \leq \frac{\Delta P}{P_{Load}} \leq 1 - \frac{V_{s,min}}{V_s} \tag{5.18}$$

Similarly, the NDZ area of reactive power is shown as the equation (5.19) shown.

$$Q_f(\frac{f_{min}}{f} - \frac{f}{f_{min}}) \leq \frac{\Delta Q}{P_{Load}} \leq Q_f(\frac{f_{max}}{f} - \frac{f}{f_{max}}) \tag{5.19}$$

NDA is shown as the following figure:

Figure 5.2
NDZ area



This experiment takes AFD (Active Frequency Detective) as example for active isnalding effect detection realization.

AFD, which effectively shrinks NDS area of passive islanding detection, is based on the theory that inverter current command injects into slight angle to make phase difference in current and voltage frequency. When it is under grid-connected status, voltage frequency is determined by power grid. When, however, power grid escapes, voltage frequency will shift due to the injection so that islanding can be detected and inverter is able to escape.

Circuit Simulation

The inverter specifications are as follows:

Inverter Specification	BUS Voltage VBUS = 100V Fs = 20kHz，Vtri = 10Vpp (PWM) CBUS = 940uF，L = 1.02mH，C = 10uF Ks = 0.3 (current sensing factor) Kv = 1/60 (AC voltage sensing factor) Kv = 1/40 (DC voltage sensing factor)

The analogue circuit diagram based on the parameters above is as the following figure 5.3 shown:
PSIM File: PEK-550_Sim5_3P_Islanding_Prot_Inv(50Hz)_ V11.1.5_V1.1

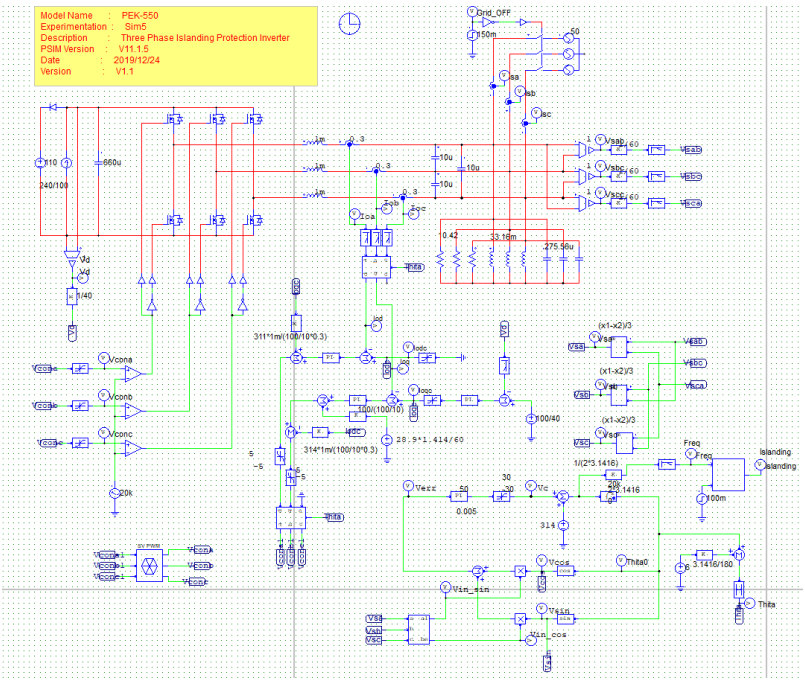


Figure 5.3 Experiment 5 PSIM analogue circuit diagram

The simulation result is shown within the figure 5.4:

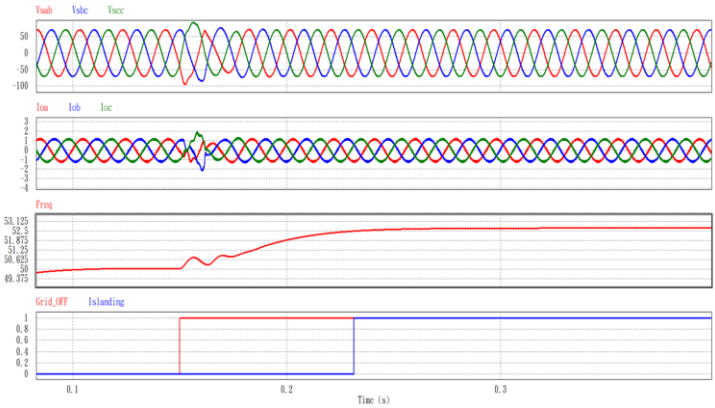


Figure 5.4 Experiment 5 analogue circuit simulation waveforms

The digital circuit diagram based on the analogue circuit is shown as the figure 5.5:

PSIM File: PEK-550_Lab5_3P_Islanding_Prot_Inv(50Hz)_V11.1.5_1.1

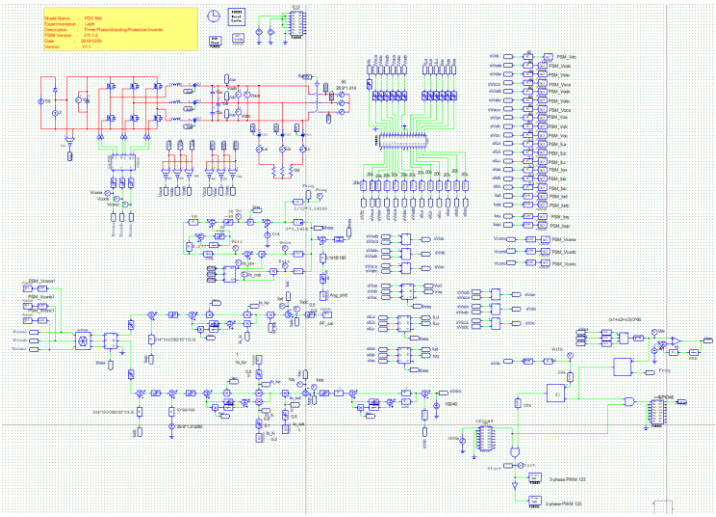


Figure 5.5 Experiment 5 PSIM digital circuit diagram

After confirming simulation, the corresponding C Code will be generated automatically via “Generate Code” of “Simulate”.

Experiment Devices

The required devices for experiment are as follows:

- PEK-550 * 1
- PEK-005A * 1
- PEK-006 * 1
- PTS-5000 * 1 (with GDS-2204E, APS-300, PSW160-7.2, GPL-500 and GPL-600)
- PC * 1

Experiment Procedure

1. The experiment wiring is shown as the figure 5.6. Please follow it to complete wiring.

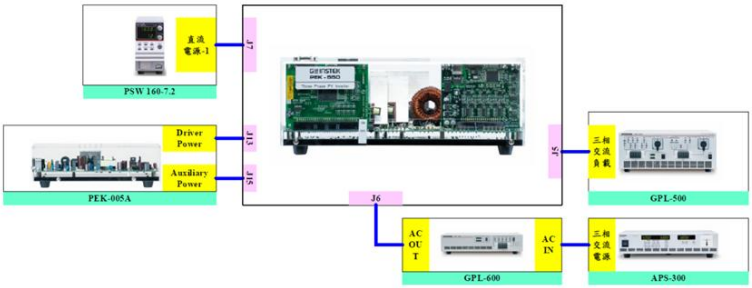


Figure 5.6 Experiment 5 wiring figure

2. After wiring, make sure the PEK-550 switch is OFF followed by turning the PEK-005A switch ON. The DSP red indicator lights on as the figure 3.13 shown, which means the DSP power is steadily normal.

Figure 5.7 DSP normal status with light on

3. Refer to the appendix B for burning procedure.
4. Connect the test leads of oscilloscope to Vo-AB, Vo-BC and Vo-CA, respectively, as the figure 5.8 shown.

Figure 5.8 Oscilloscope test leads wiring

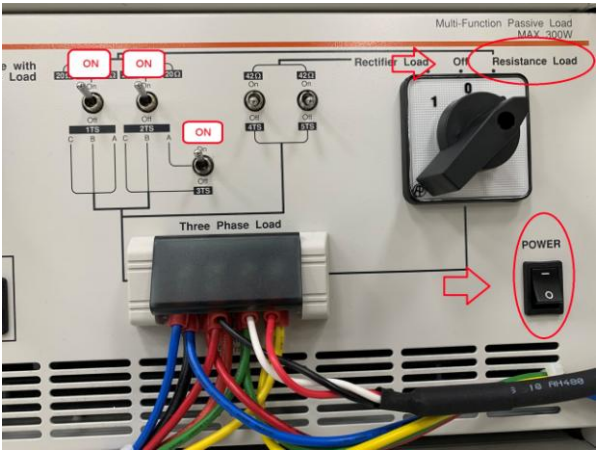
5. Set voltage as 110V, current as 2A for PSW160-7.2 as the figure 5.9 shown.

Figure 5.9 The settings of PSW 160-7.2

6. As the figure 5.10 shown, follow the steps below for GPL-500 operation. Power on GPL-500 → Rotate the Three Phase Lord knob to Resistance Load → Set 1TS and 2TS and 3T as ON, which indicates full-load mode.

Figure 5.10

The full-load setting of GPL-500

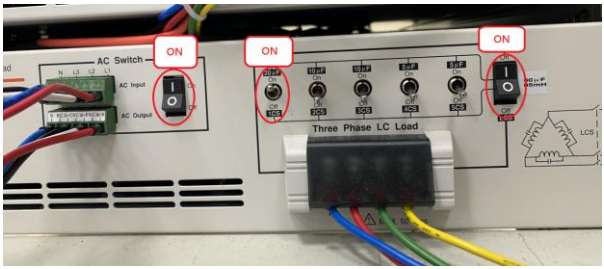


7. The operation process of APS-300 is shown as the figure 5.11. Power on APS-300 → Set 50Hz for frequency → Set operation mode as 3P4W → Set output voltage as 28.86V.

Figure 5.11
APS-300 Settings

8. After setting, turn on both PSW and APS-300 power output followed turning on PEK-550. And after turning on LCS switch of GPL-600, both GPL-600 and GPL-500 will be in parallel (cords of in parallel have been connected between GPL-500 and GPL-600 beforehand in PTS-5000 system). Further turn on 1CS(20uF) of the adjusted capacitor and also turn on the AC switch as the figure 5.12 shown.

Figure 5.12



9. After setting up, turn on PSW and APS-300 power output followed by powering on PEK-550 for test.

The experiment result

- When PEK-550 is turned on, it has seen that power provided by PSW is 200W and also single phase 26.6W in power provided by APS-300 as the figure 5.13 shown.

Figure 5.13

(a) PSW (b) APS-300 output power

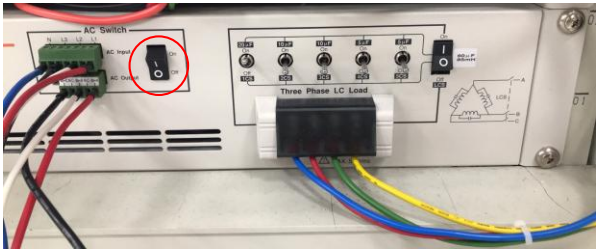
In order to build islanding effect, it is required to modify output power of inverter via PSW output current adjustion to result in zero for APS-300 output power as the figure 5.14 shown. The figure 5.15 shows that AC switch of GPL-600 is cut off.

Figure 5.14

APS-300 output power is zero

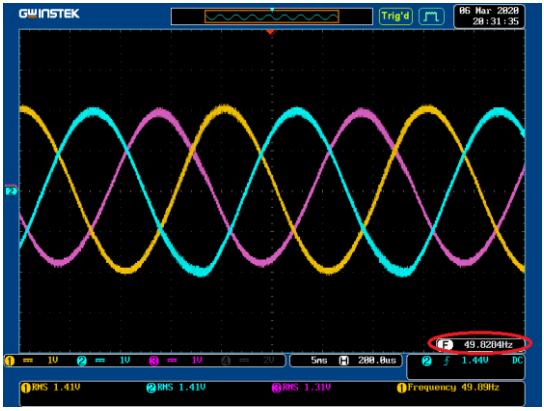
Figure 5.15

APS-300 cut-off method



- If PEK-550 maintains operation after AC switch is cut off, it signals that the harmonic frequency formed by system is 49.8Hz. and inverter is not able to detect that grid power has been cut off and thus keep its operation, which is known as islanding effect as the figure 5.16 shown.

Figure 5.16 Output voltage frequency under islanding effect



- If PEK-550 escapes immediately after AC switch is cut off, it is because that harmonic frequency formed by system is not within the set range. Therefore, it is necessary to turn off PEK-550, PSW and APS-300 altogether followed by rebooting AC switch and restore back to the step 8 of experiment. Also, it is required to fine tune the capacitors in parallel of GPL-600 as the figure 5.17 shown. In addition to the original 1CS(20uF), please connect the 5CS(5uF) in parallel as well and repeat the following steps until AC switch is cut off and PEK-550 no longer escapes.

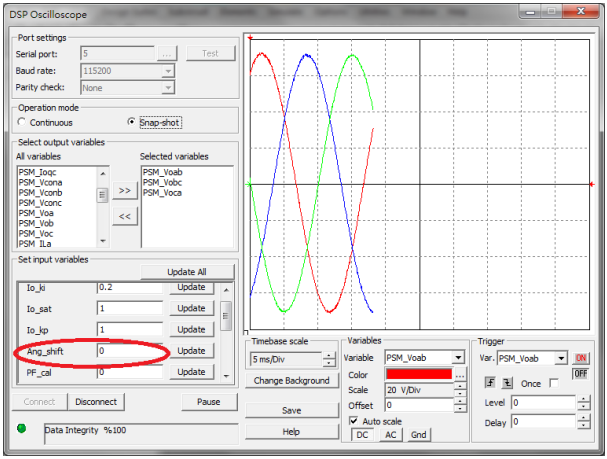
Figure 5.17 Fine tune load capacitor (in parallel 5uF)

- After islanding effect is established, it is available to, from oscilloscope, observe that the current output voltage frequency

is 49.8Hz.Through the AFD method, adjust current shift angle (0 degree by default) via RS232 as the figure 5.18 shown.

Figure 5.18

Adjust shift angle in PSIM (Ang_shift)



1. When adjusting shift angle to 1, output voltage frequency will be 50.3Hz as the figure 5.19 shown. When adjusting shift angle to 2, output voltage frequency will be 50.8Hz as the figure 5.20 shown. When adjusting shift angle to 3, PEK-550 will escape immediately.
2. When adjusting shift angle to -1, voltage frequency will be 49.3Hz as the figure 5.21 shown. When adjusting shift angle to -2, PEK-550 will escape immediately.

Figure 5.19

The output voltage frequency when shift angle is 1

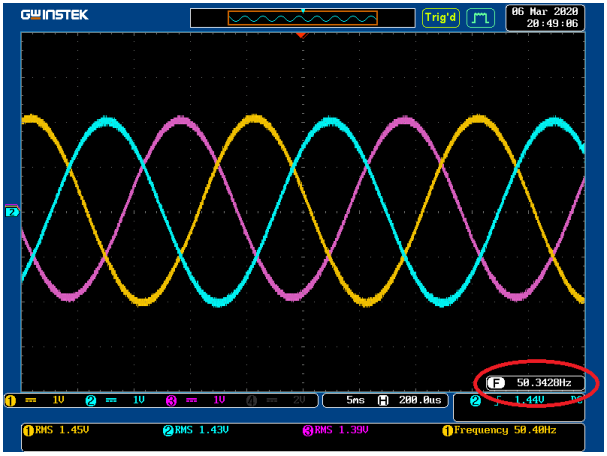


Figure 5.20

The output voltage frequency when shift angle is 2

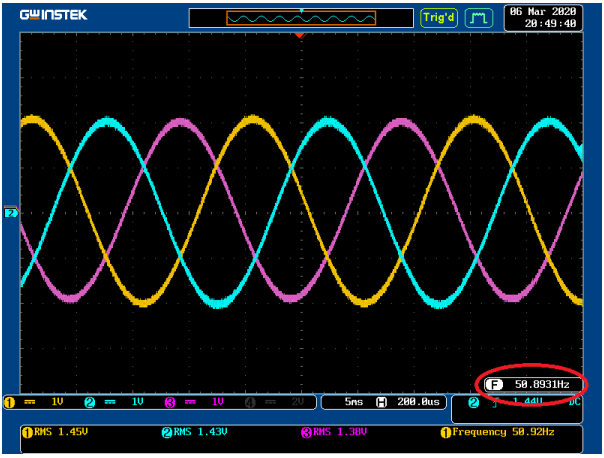
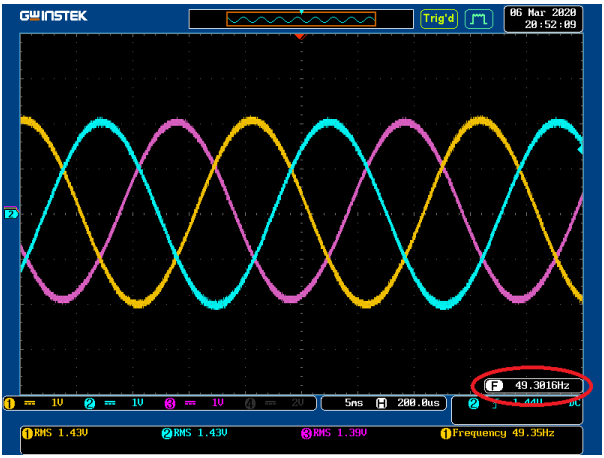


Figure 5.21

The output voltage frequency when shift angle is -1



Fill in the table 5.4 with the varied shift angles and relative voltage frequencies.

Table 5.4 Shift angle and output frequency

Shift Angle	Output Voltage Frequency (Hz)
0	49.8
1	50.3
2	50.8
-1	49.3

From the table 5.4, it has seen that when shift angle deviates from 0, the output voltage frequency will be farther away from 50Hz. PEK-550 will escape when output voltage frequency is not within the range of 52.5Hz and 47.5Hz. If setting the system shift angle as 3, islanding effect will be detected automatically and PEK-550 will escape.

Experiment 6 – Three Phase PV Grid-connected Inverter

Preview

1. Understand MPPT boost converter and full system operation after combination of grid power in parallel and inverter
2. Learn the second-stage circuit start method
3. Validate MPPT under the second-stage circuit system
4. Validate the power grid in parallel under the second-stage circuit system
5. Learn analog circuit establishment and simulation
6. Learn DSP digital control circuit plan

Experiment Content and Purpose

1. Learn operation of the second-stage PV inverter system

Principle and Design

This experiment is the second-stage grid power in parallel inverter circuit and its control architecture is shown as the figure 6.1. Of the circuit, boost converter controls input voltage in order to reach the MPPT purpose of PV panel. The three phaser inverter, on the other hand, maintains BUS DV voltage stability and takes advantage of phase lock loop to reach synchronization between inverter and grid

power. Refer to the experiment 4 for the boost circuit design and the experiement 3 for the three phase inverter circuit design.

The start sequence indicates that relay grid connection is lauched when phase lock loop synchronizes with grid power. After grid connection, make sure DC side BUS voltage and lauch inverter PWM followed by turning on boost circuit PWM.

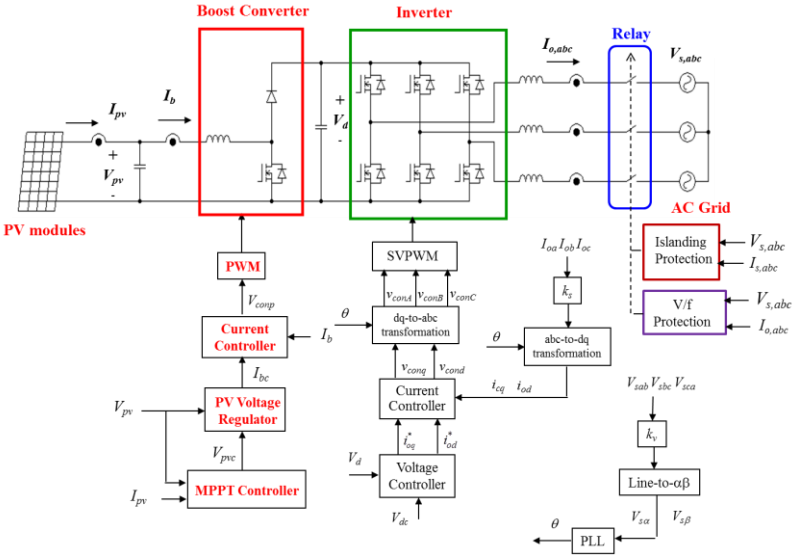


Figure 6.1 Circuit control architecture

Circuit Simulation

The specification of inverter is as follows:

Inverter Specification	Input Voltage Vb = 70V
	BUS Voltage Vd = 100V
	AC Source Voltage VLL = 50Vrms
	Fs = 40kHz，Vm = 5Vpp (Boost PWM)
	Fs = 20kHz，Vtri = 10Vpp (Inverter PWM)
	Cb = 200uF，Lb = 660uH
	CBUS = 940uF，L = 1.02mH，C = 10uF
	Ks = 0.3 (AC current sensing factor)
	Ks = 0.6 (DC current sensing factor)
	Kv = 1/60 (AC voltage sensing factor)
	Kv = 1/40 (DC voltage sensing factor)

The analogue circuit diagram based on the parameters above is as the following figure 6.2 shown:
PSIM File: PEK-550_Sim6_3P_PV_GC_Inv(50Hz)_V11.1.5_V1.1

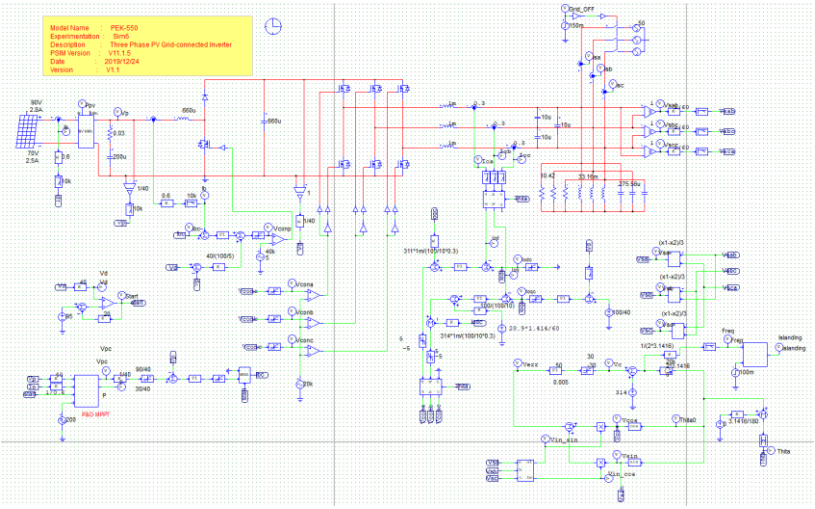


Figure 6.2 Experiment 6 PSIM analogue circuit diagram

The simulation result is shown within the figure 6.3:

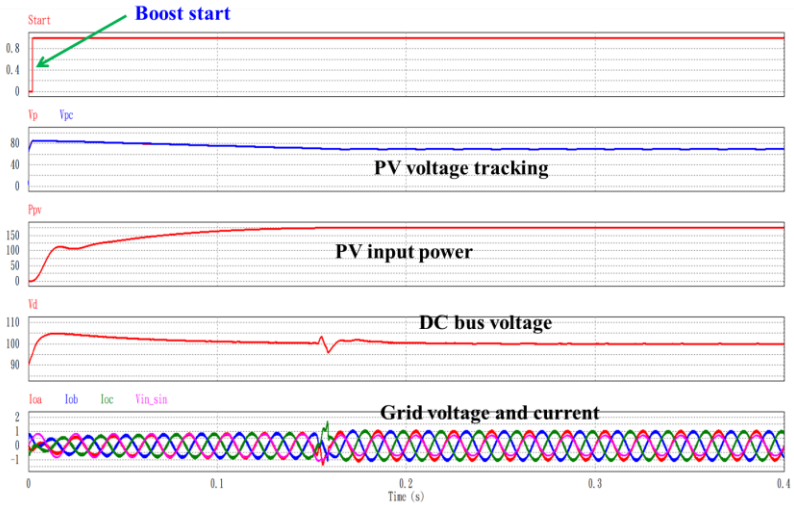


Figure 6.3 Experiment 6 analogue circuit simulation waveforms

The digital circuit diagram based on the analogue circuit is shown as the figure 6.4:
PSIM File: PEK-550_Lab6_3P_PV_GC_Inv(50Hz)_V11.1.5_V1.1

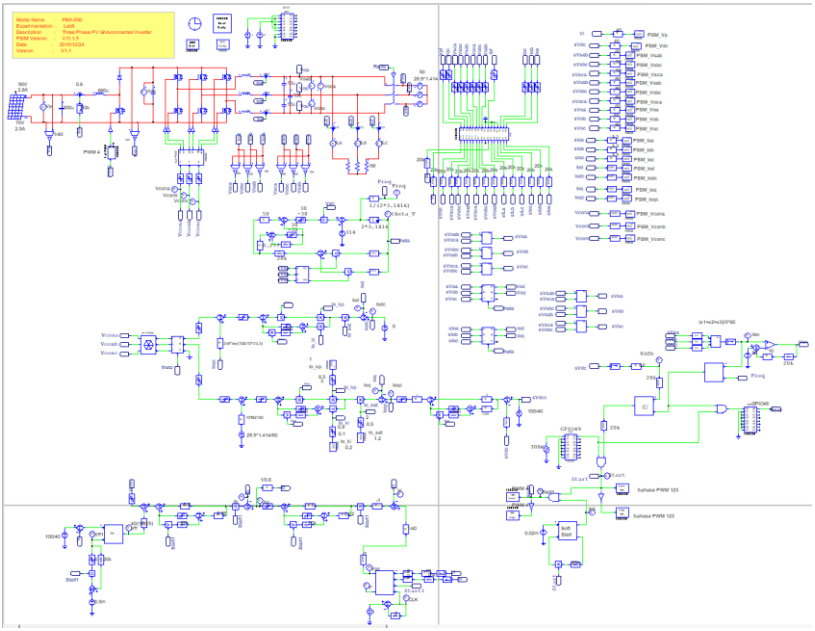


Figure 6.4 Experiment 6 PSIM digital circuit diagram

Because the circuit, which practically generates Code, has the MPPT adjusted frequency 2Hz and it is time-consuming for simulation based on this circuit file, we alternately provide another digital circuit, "PEK-550_Sim6D_3P_PV_GC_Inv(50Hz)_V11.1.5_V1.1", of MPPT adjusted frequency 100Hz, based on which it requires relatively shorter period for simulation result. Refer to the figure 6.5 for the simulation result.

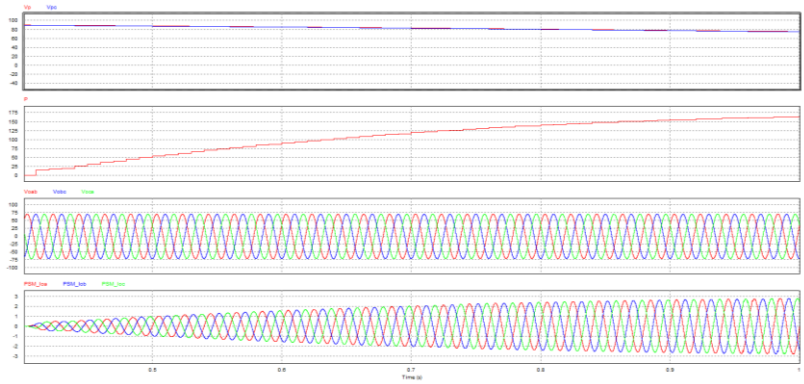


Figure 6.5 Experiment 6 digital circuit simulation waveforms

After confirming simulation, the corresponding C Code will be generated automatically via “Generate Code” of “Simulate”.

Experiment Devices

The required devices for experiment are as follows:

- PEK-550 * 1
- PEK-005A * 1
- PEK-006 * 1
- PTS-5000 * 1 (with GDS-2204E, APS-300, PSW160-7.2, APS-300 and GPL-500)
- PC * 1

Experiment Procedure

1. The experiment wiring is shown as the figure 6.6. Please follow it to complete wiring.

Figure 6.6 Experiment 6 wiring figure

2. After wiring, make sure the PEK-550 switch is OFF followed by turning the PEK-005A switch ON. The DSP red indicator lights on as the figure 3.7 shown, which means the DSP power is steadily normal.

Figure 6.7 DSP normal status with light on

3. Refer to the appendix B for burning procedure.
4. Connect the test leads of oscilloscope to Vo-AB, Vo-BC and Vo-CA, respectively, as the figure 6.8 shown.

Figure 6.8 Oscilloscope test leads wiring

5. Refer to the appendix D – SAS software operation manual for PV system setting process in simulation. As the figure 6.9 shown, the open circuit voltage of first curve is 90V, and the short circuit current is 2.8A with the MPP voltage 70V along with the MPP current 2.5A. As the figure 6.10 shown, the value of second curve is set 90% of the first curve MPP. The open circuit voltage of the second curve MPP, therefore, is 81V, and the short circuit current is 2.52A with the MPP voltage 63V along with the MPP current 2.25A.

Figure 6.9

The 1st curve setting value

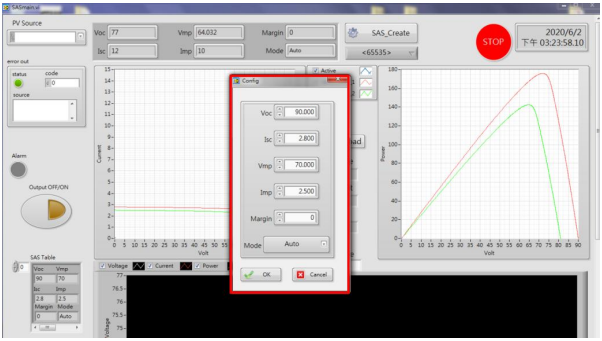
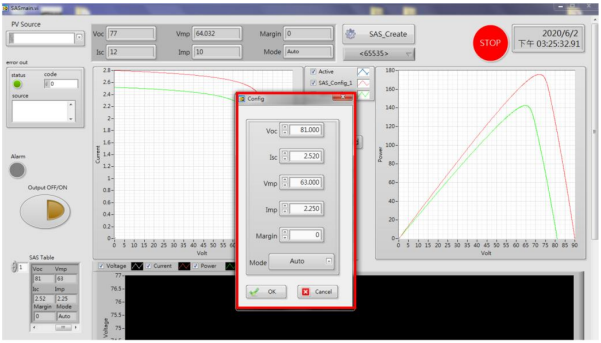


Figure 6.10
The 2nd curve setting value

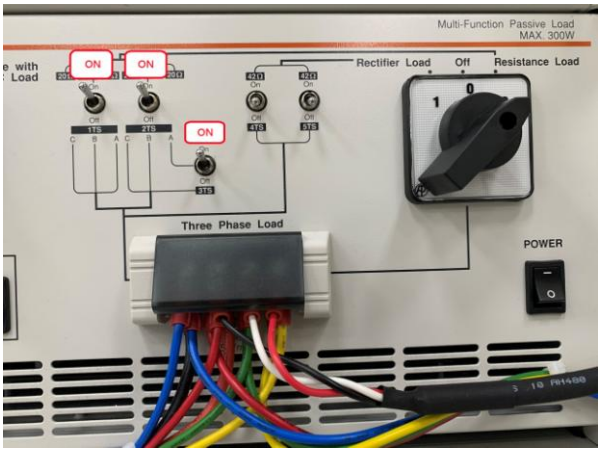


6. As the figure 6.11 shown, power on APS-300 and set 50Hz for frequency, 3P4W for mode, 28.86V for output voltage.

Figure 6.11
The setting of APS-300

7. As the figure 6.12 shown, power on GPL-500 and rotate the Three Phase Load knob to Resistance Load. Set 1TS, 2TS and 3TS as ON, which indicates the full-load mode.

Figure 6.12
GPL-500 full-load setting



8. After setting up, turn on PSW power output followed by powering on PEK-550 for test.

The purpose of experiment

When PEK-550 phase lock is completed, relay starts up and PEK-550 is grid-connected with APS-300. It has seen that APS-300 begins providing/absorbing power and PSW output voltage is approaching MPPT point.

Through the experiment process, the default 2 different PV curves, which are used to simulate the varied curves generated by differd sun exposure, can be switched at any time and will approach the MPPT point in the end, respectively, as the figure 6.13 and 6.14 shown.

Figure 6.13

SAS in the maximum power point of the 1st curve

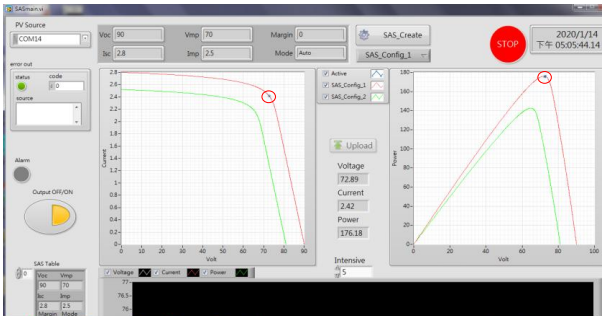
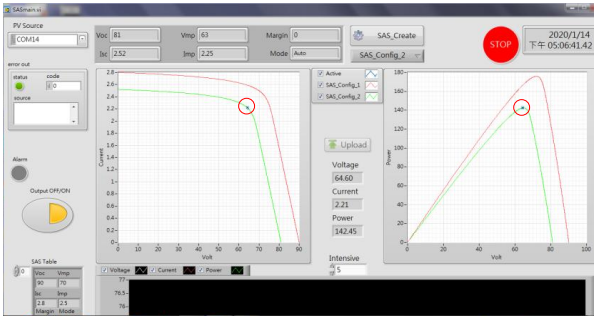


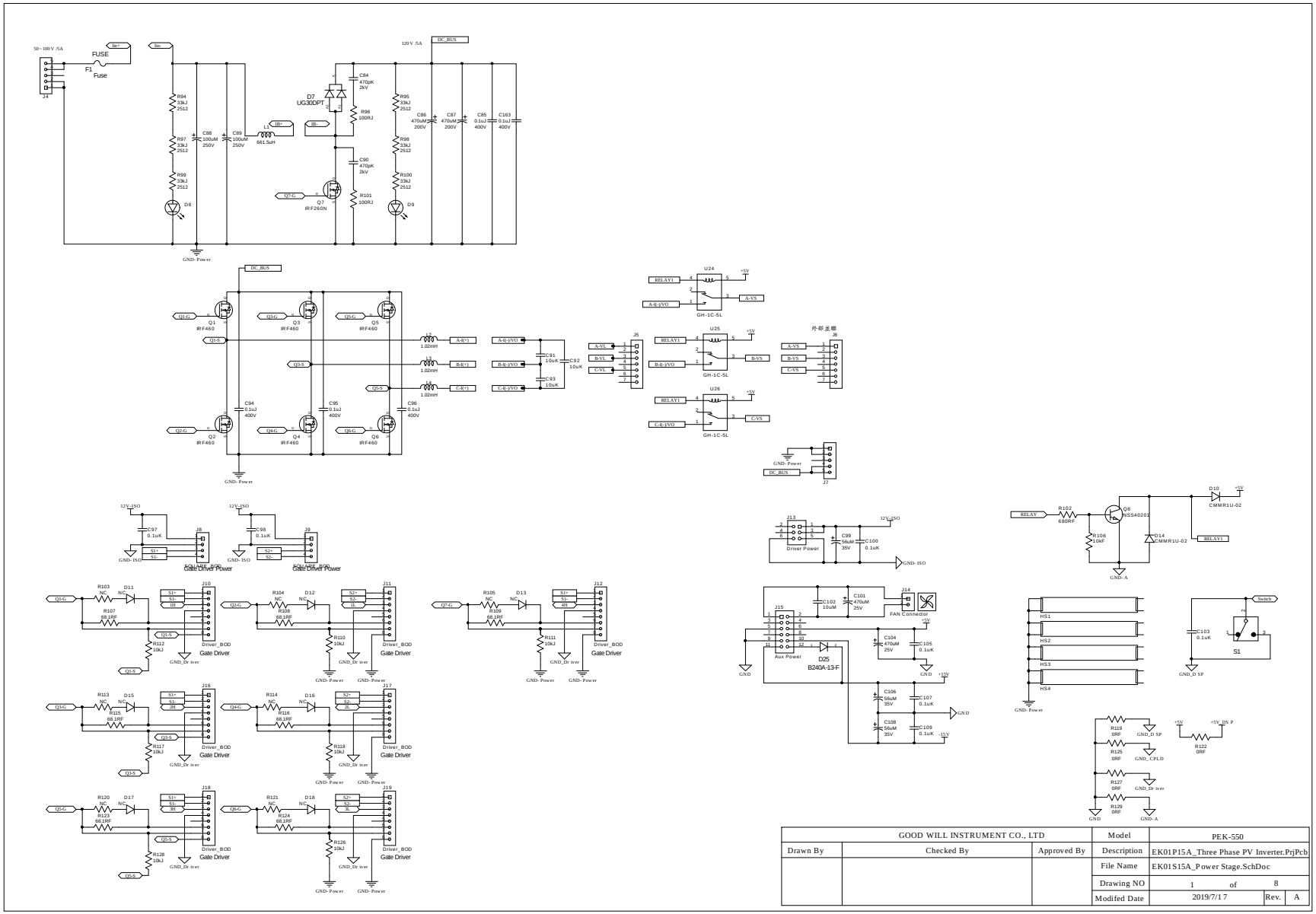
Figure 6.14

SAS in the maximum power point of the 2nd curve

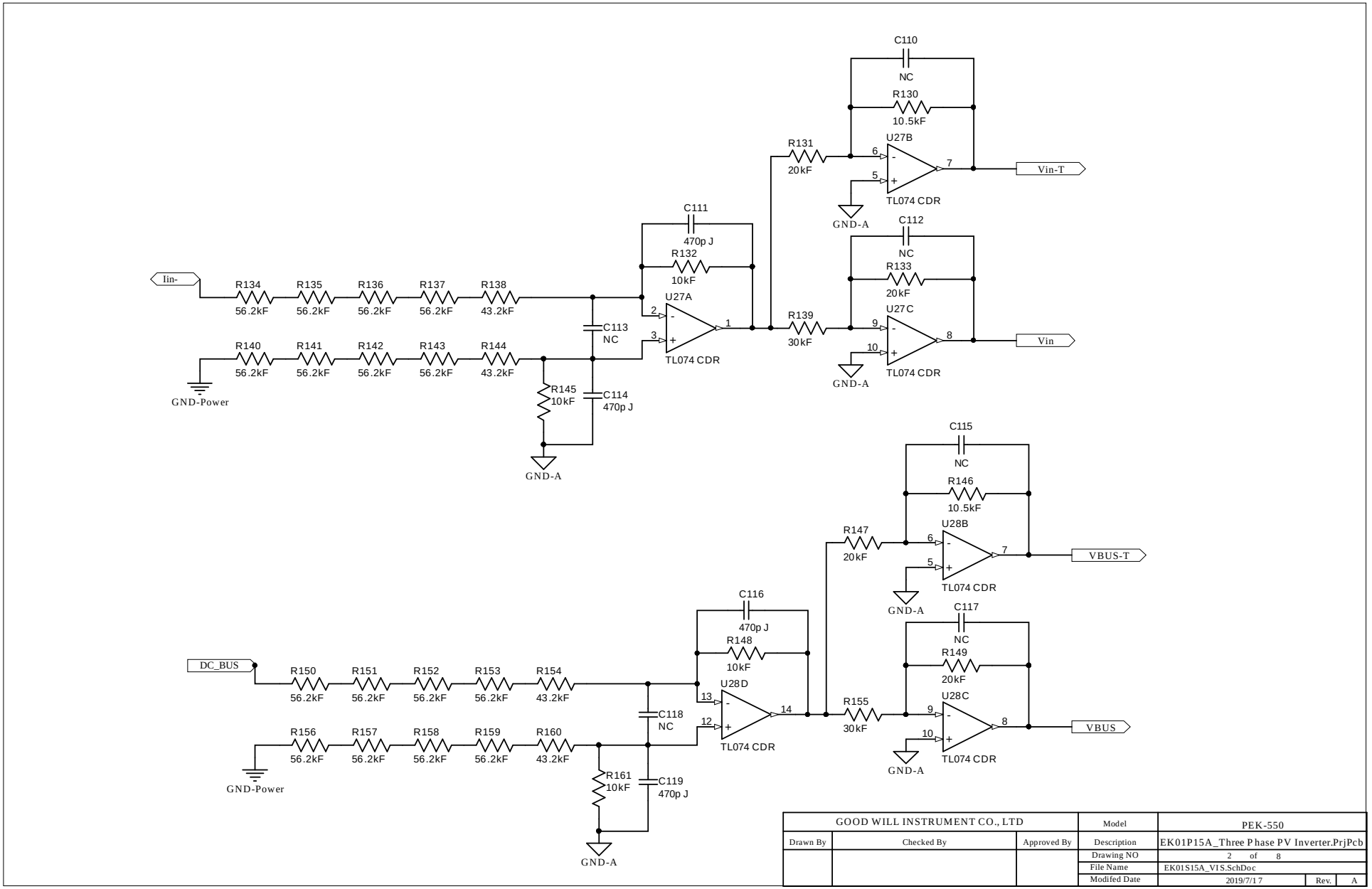


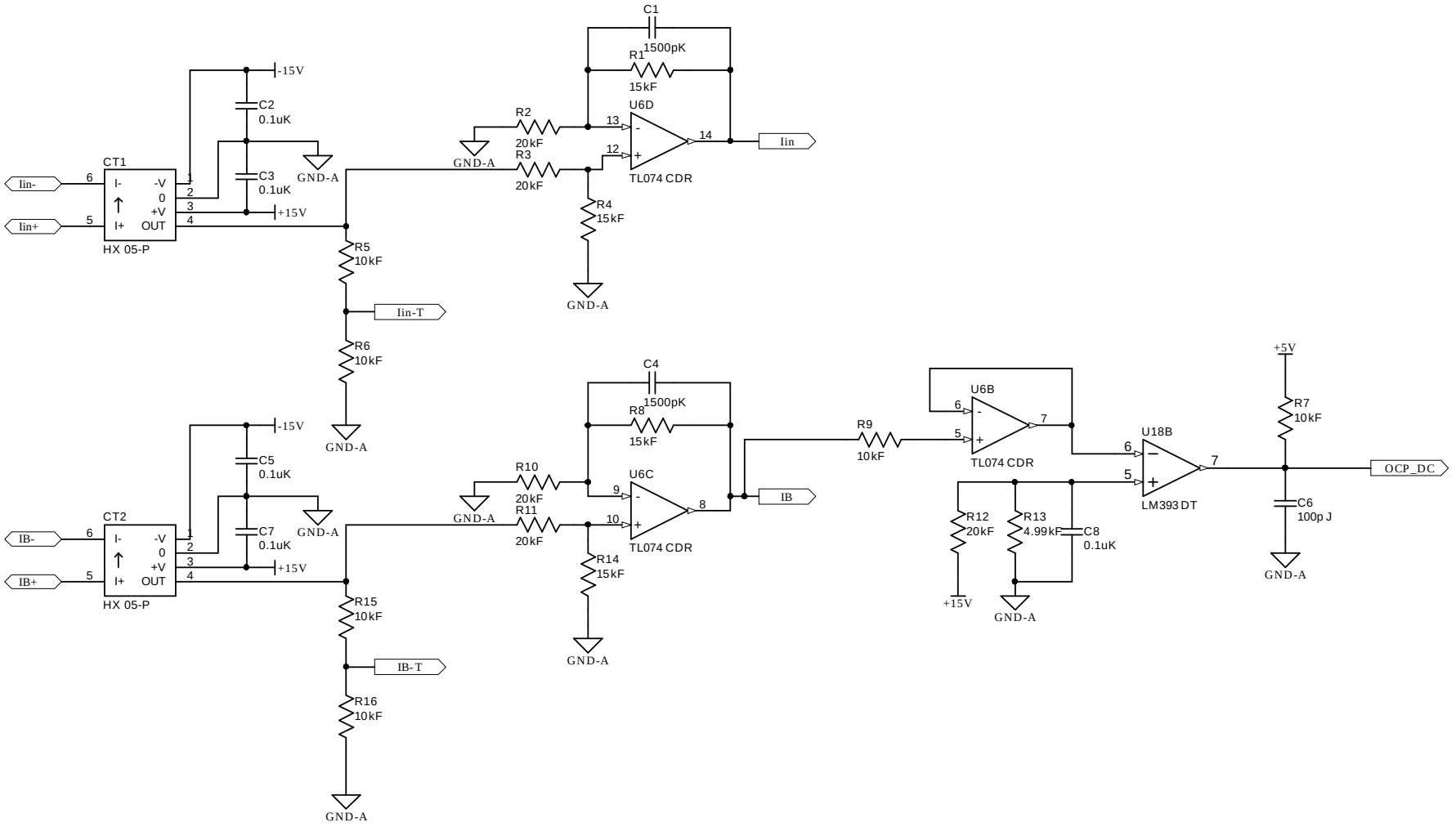
Appendix A – PEK-550 Circuit Diagram

Three Phase Inverter

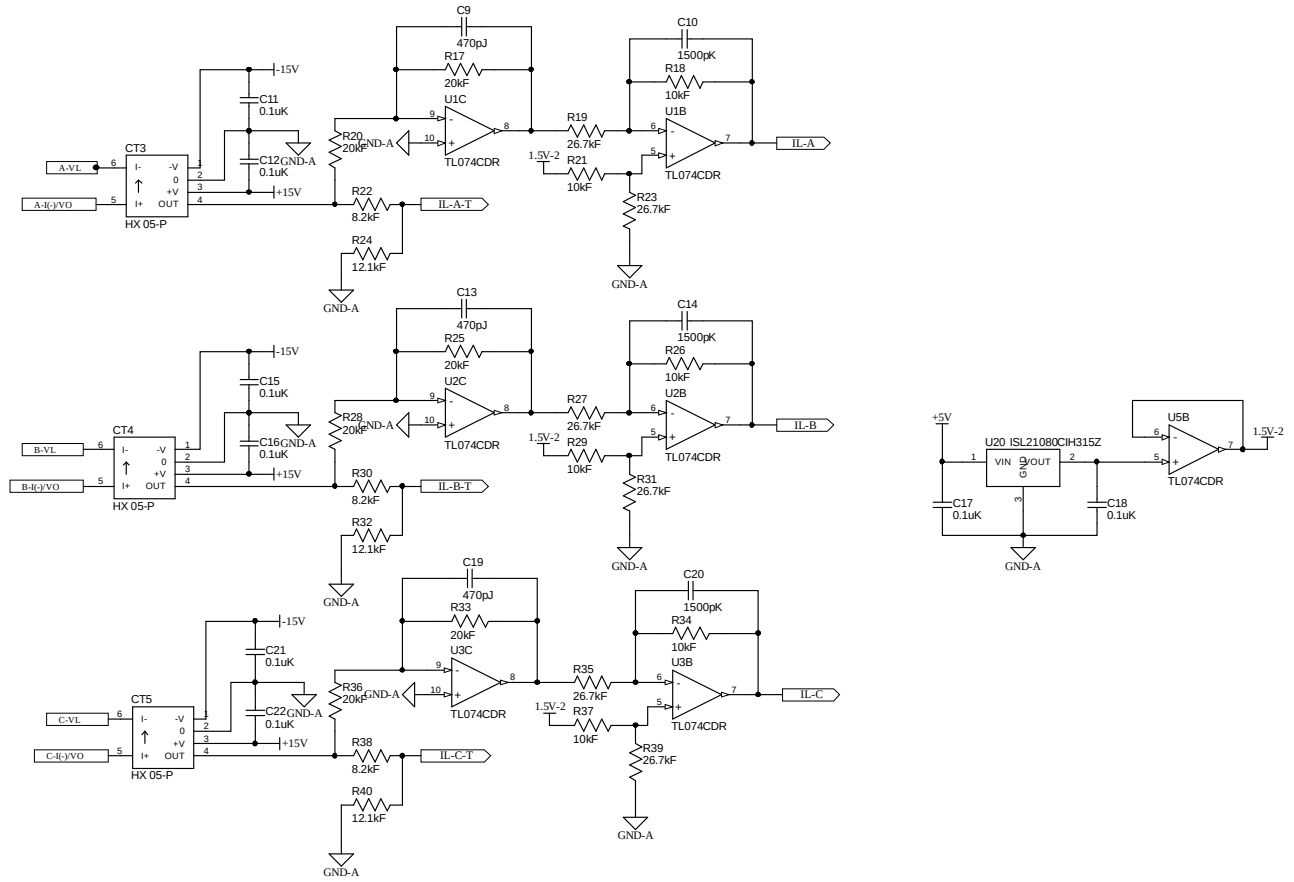


GOOD WILL INSTRUMENT CO., LTD			Model	PEK-550
Drawn By	Checked By	Approved By	Description	EK01P15A_Three Phase PV Inverter.PrjPcb
			File Name	EK01S15A_Power Stage.SchDoc
			Drawing NO	1 of 8
			Modifed Date	2019/7/17 Rev. A

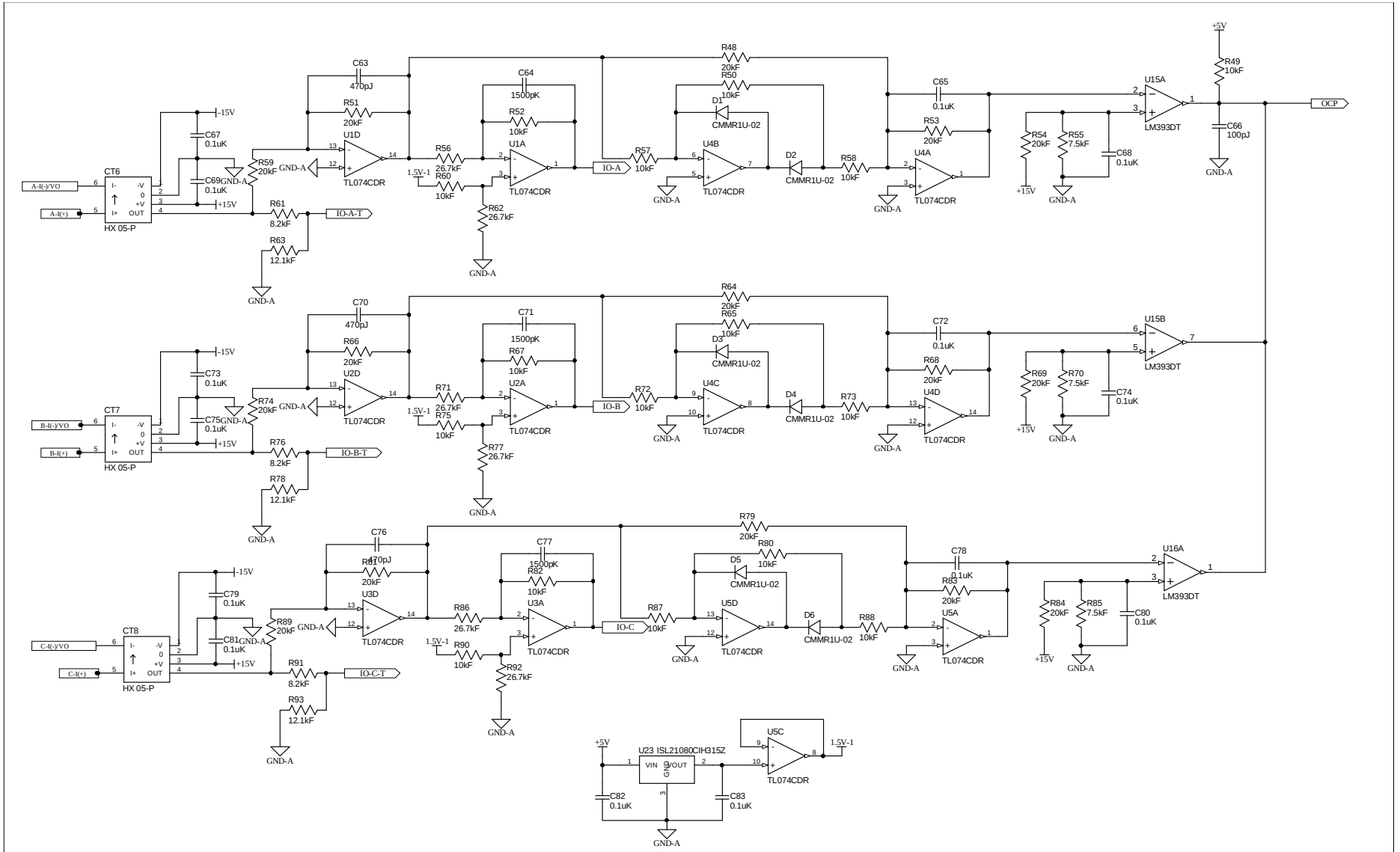

C110
NC
R130
10.5kF
R131
20kF
U27B
TL074 CDR
Vin-T
GND-A
C111
470p J
R132
10kF
C112
NC
R133
20kF
Iin-
R134 R135 R136 R137 R138
56.2kF
U27A
C113
NC
R139
30kF
U27C
Vin
R140 R141 R142 R143 R144
43.2kF
R145
10kF
C114
470p J
GND-Power
C115
NC
R146
10.5kF
R147
20kF
U28B
VBUS-T
C116
470p J
C117
NC
R148
10kF
R149
20kF
DC_BUS
R150 R151 R152 R153 R154
U28D
U28C
C118
NC
R155
30kF
VBUS
R156 R157 R158 R159 R160
R161
10kF
C119
470p J
GOOD WILL INSTRUMENT CO., LTD
Model
PEK-550
Drawn By
Checked By
Approved By
Description
EK01P15A_Three Phase PV Inverter.PrjPcb
Drawing NO
2 of 8
File Name
EK01S15A_V1S.SchDoc
Modifed Date
2019/7/17
Rev.
A



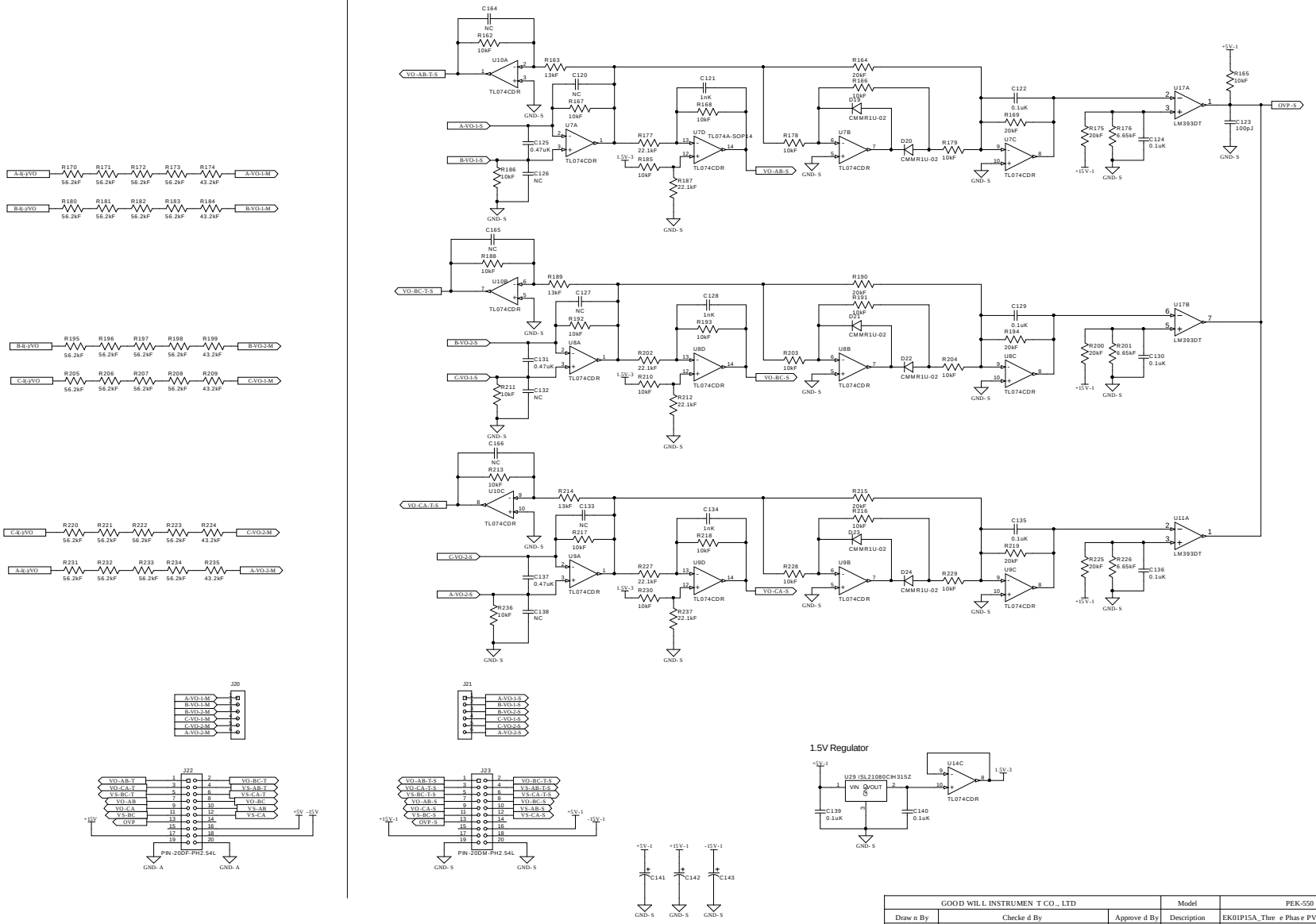
GOOD WILL INSTRUMENT CO., LTD			Model	PEK-550
Drawn By	Checked By	Approved By	Description	EK01P15A_Three Phase PV Inverter.PrjPcb
			Drawing NO	3 of 8
			File Name	EK01S15A_IIS.SchDoc
			Modifed Date	2019/7/17 Rev. A



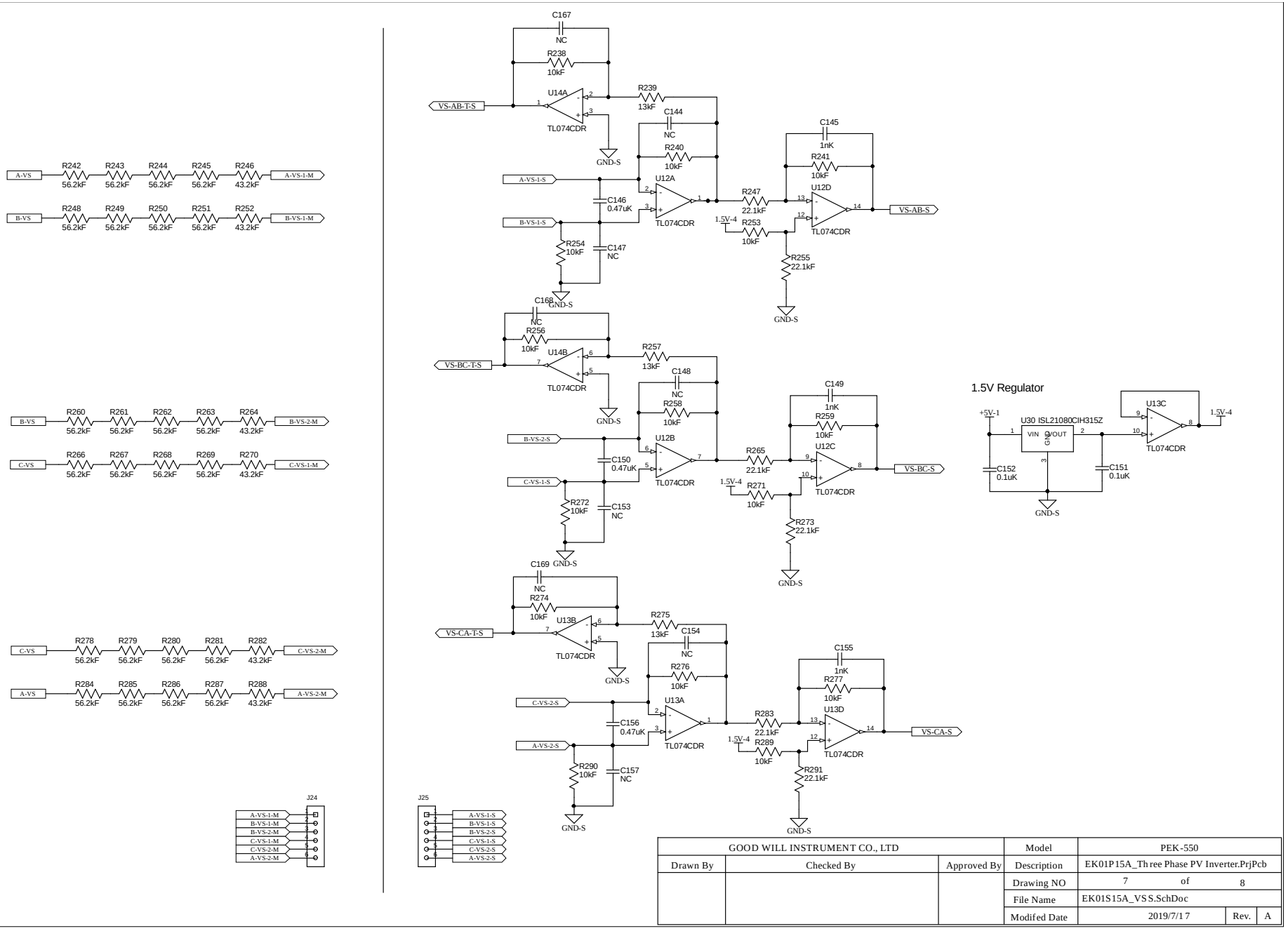
GOOD WILL INSTRUMENT CO., LTD			Model	PEK-550		
Drawn By	Checked By	Approved By	Description	EK01P15A_Three Phase PV Inverter.PrjPcb		
			Drawing NO	4 of 8		
			File Name	EK01S15A_ILS.SchDoc		
			Modifed Date	2019/7/17	Rev.	A



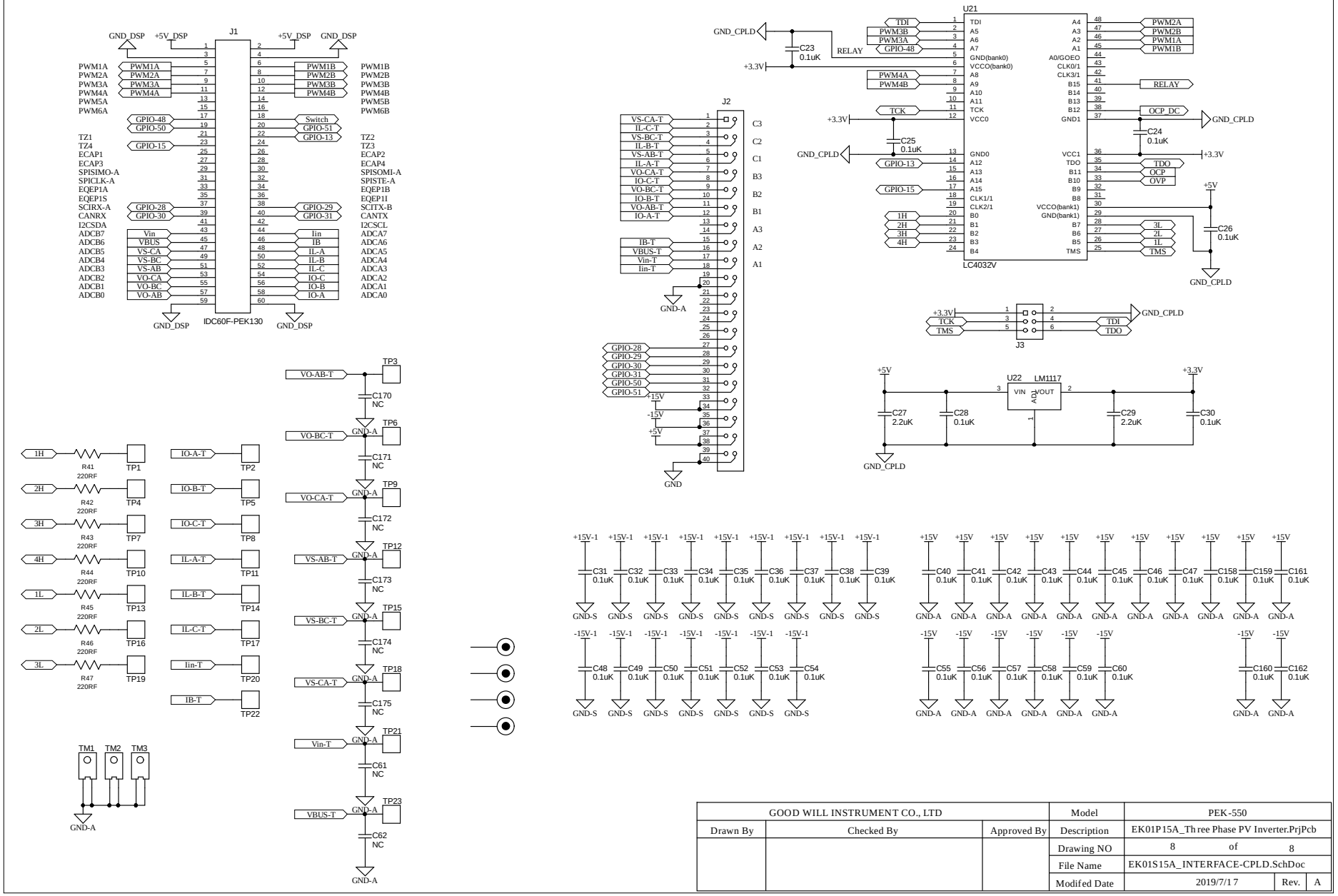
GOOD WILL INSTRUMENT CO., LTD			Model	PEK-550	
Drawn By	Checked By	Approved By	Description	EK01P15A_Three Phase PV Inverter.PrjPcb	
			Drawing NO	5 of 8	
			File Name	EK01S15A_IOS-OCP.SchDoc	
			Modifed Date	2019/7/17	Rev. A



GOOD WILL INSTRUMEN T CO., LTD			Model	PEK-550
Draw n By	Checke d By	Approve d By	Description	EK01P15A_Thre e Phas e PV Inverte r.PrjPcb
			Drawin g NO	6 of 8
			File Name	EK01S15A_VOS-OV P.SchDoc
			Modife d Date	2019/7/17 Rev. A

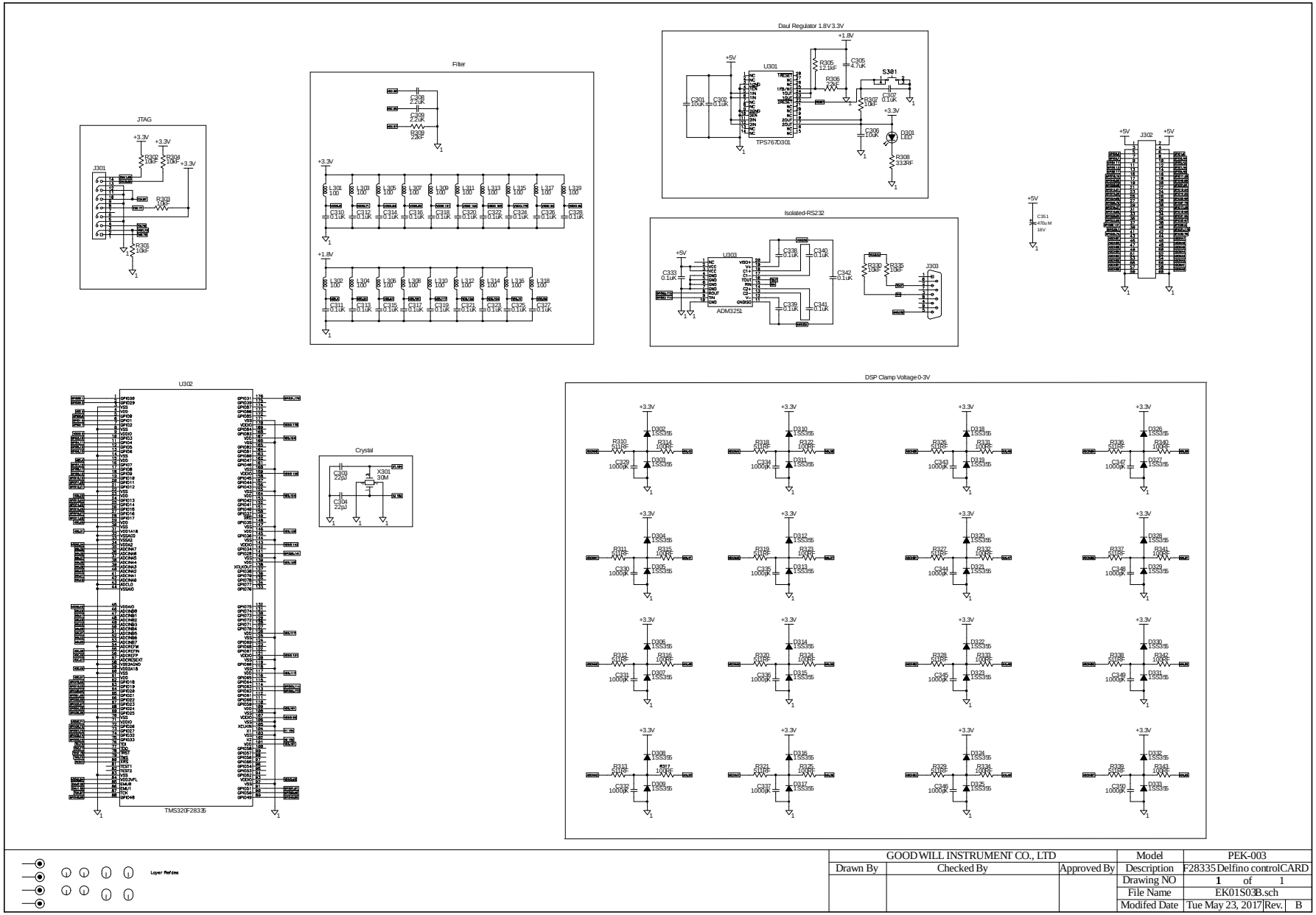


GOOD WILL INSTRUMENT CO., LTD			Model	PEK-550
Drawn By	Checked By	Approved By	Description	EK01P15A_Three Phase PV Inverter.PrjPcb
			Drawing NO	7 of 8
			File Name	EK01S15A_VSS.SchDoc
			Modifed Date	2019/7/17 Rev. A

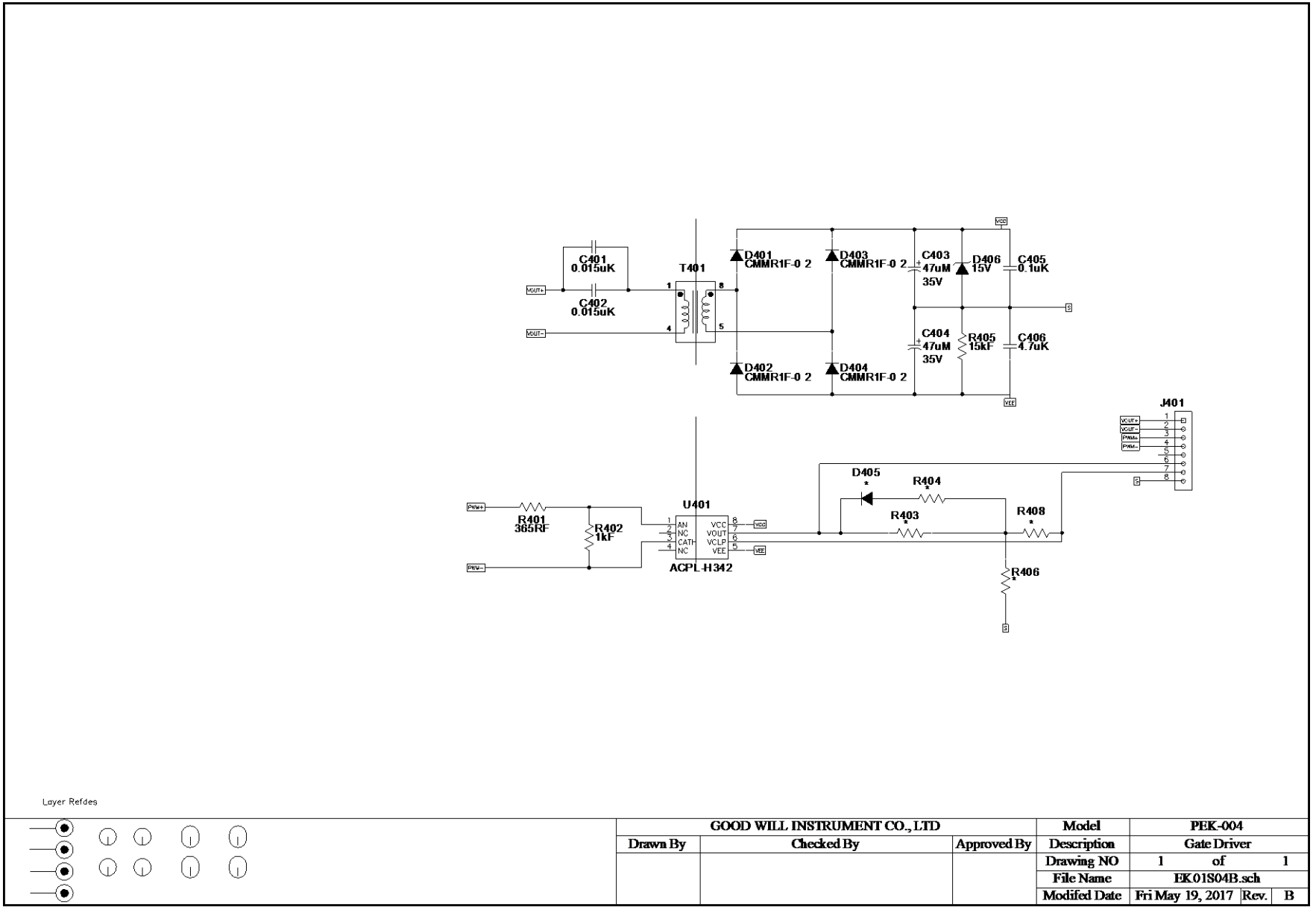


GOOD WILL INSTRUMENT CO., LTD			Model	PEK-550	
Drawn By	Checked By	Approved By	Description	EK01P15A_Three Phase PV Inverter.PrjPcb	
			Drawing NO	8 of 8	
			File Name	EK01S15A_INTERFACE-CPLD.SchDoc	
			Modifed Date	2019/7/17	Rev. A

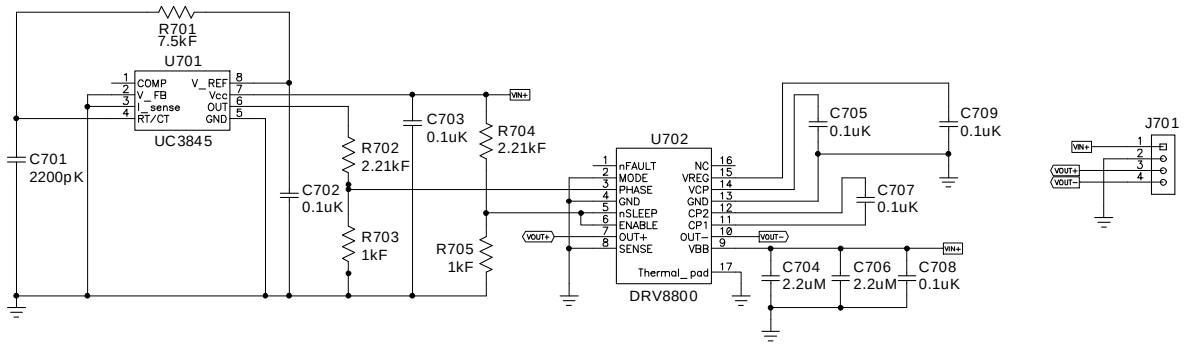
F28335 Delfino control CARD



Gate Driver


C401
0.015uK
C402
0.015uK
T401
D401
CMMR1F-0 2
D403
CMMR1F-0 2
D402
CMMR1F-0 2
D404
CMMR1F-0 2
C403
47uM
35V
C404
47uM
35V
D406
15V
C405
0.1uK
R405
15kF
C406
4.7uK
J401
D405
R404
R403
R408
R406
R401
365RF
R402
1kF
U401
ACPL-H342
Layer Refdes
GOOD WILL INSTRUMENT CO., LTD
Drawn By
Checked By
Approved By
Model
PEK-004
Description
Gate Driver
Drawing NO
1 of 1
File Name
EK01S04B.sch
Modifed Date
Fri May 19, 2017
Rev.
B

Gate Driver Power



Layer Refdes

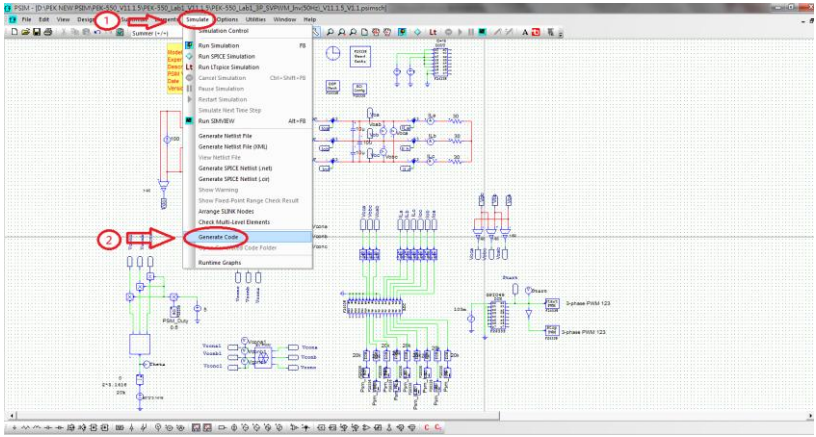
GOOD WILL INSTRUMENT CO., LTD			Model	PEK-100	
Drawn By	Checked By	Approved By	Description	Gate Driver Power	
			Drawing NO	1 of 1	
			File Name	EK01S07A.sch	
			Modifed Date	Mon Mar 09, 2015	Rev. A

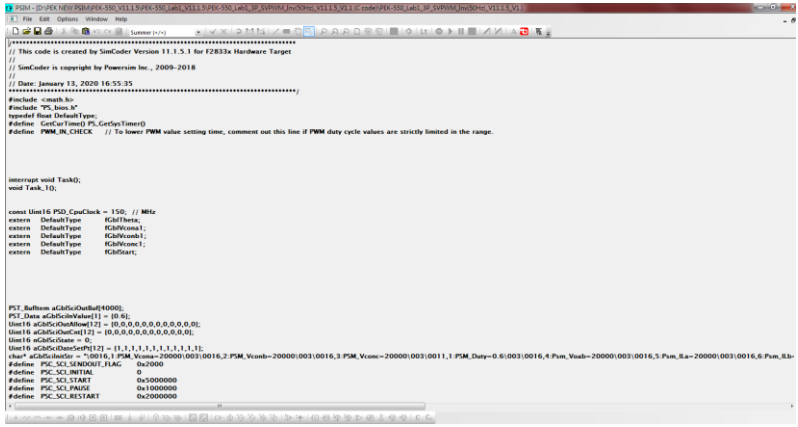
Appendix B – C Code Burning Procedure

This appendix takes "PEK-550_Lab1_3P_SVPWM_Inv(50Hz)_V11.1.5_V1.1" as an example for the instruction. See the detailed steps below.

Operating steps

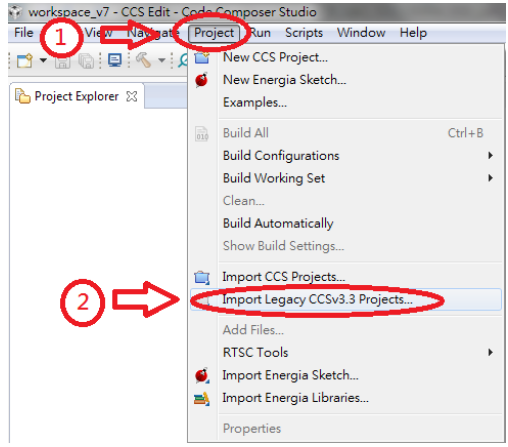
1. Open the digital circuit file "PEK-550_Lab1_3P_SVPWM_Inv(50Hz)_V11.1.5_V1.1" within the PSIM program followed by clicking "Generate Code" from "Simulate" tab. The PSIM will generate C Code automatically as shown below.



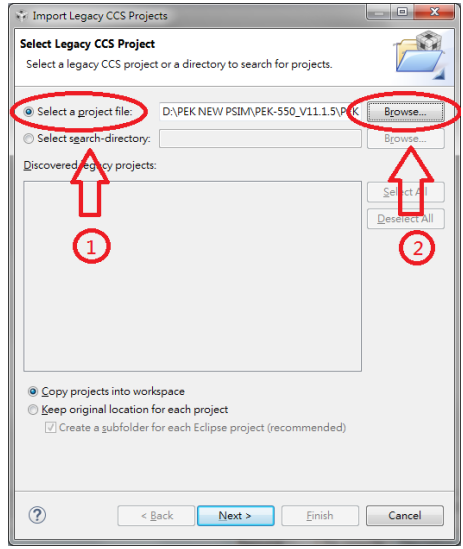


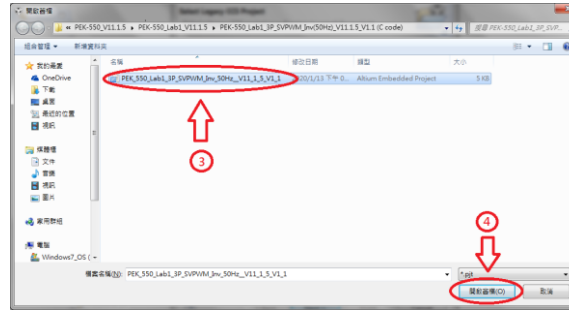
2. A folder of identical name with the PSIM circuit file in which the required files for burning and C Code are well saved will be generated in the location of PSIM circuit file by system.

3. Open CCS and select “Project” tab followed by clicking ”Import Legacy CCSv3.3 Projects” as the figure below.

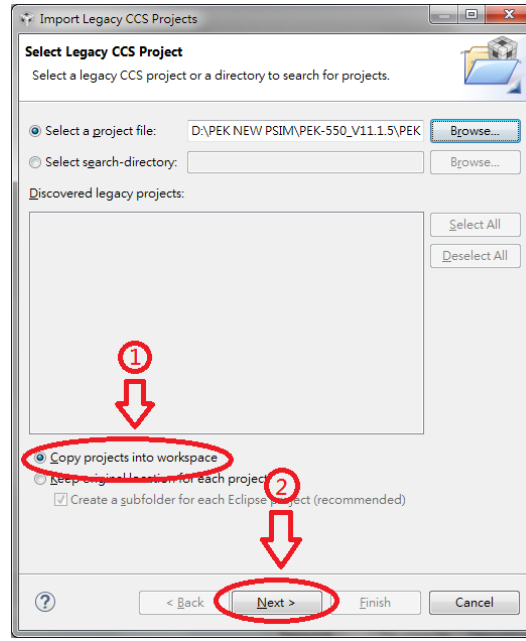


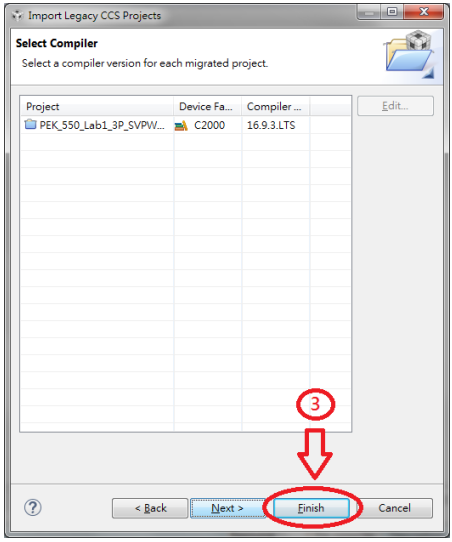
4. Go to "Select a project file" and click "Browser" followed by searching the folder where C Code is located and selecting the file with name extension ".pjt" as the following figure shown.

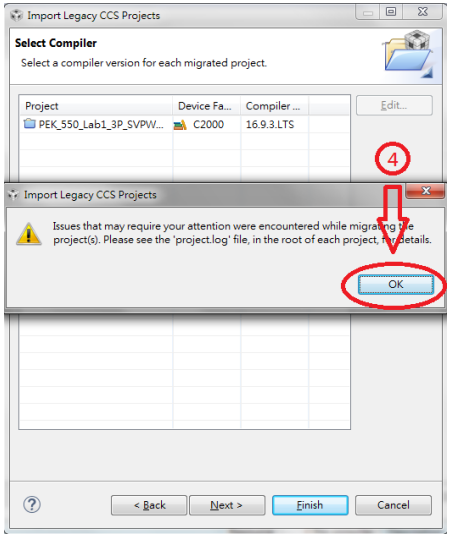




5. Select " Copy projects into workspace " followed by clicking "Next" and then "Finish" to import C Code into CCS program. See the figure below.




Import Legacy CCS Projects
Select Compiler
Select a compiler version for each migrated project.
Project
Device Fa...
Compiler ...
PEK_550_Lab1_3P_SVPW...
C2000
16.9.3.LTS
Edit...
3
< Back
Next >
Finish
Cancel


Import Legacy CCS Projects
Select Compiler
Select a compiler version for each migrated project.
Project
Device Fa...
Compiler ...
PEK_550_Lab1_3P_SVPW...
C2000
16.9.3.LTS
Edit...
4
Import Legacy CCS Projects
Issues that may require your attention were encountered while migrating the project(s). Please see the 'project.log' file, in the root of each project, for details.
OK
< Back
Next >
Finish
Cancel

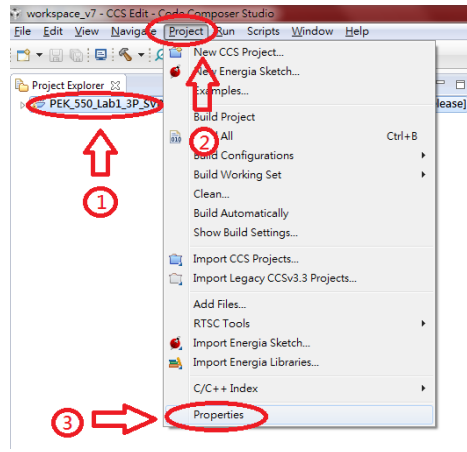
6. Select C Code file and choose "Properties" from "Project" tab. The setting steps are as follows.

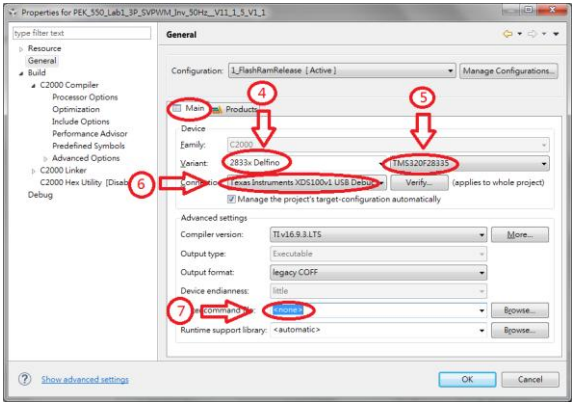
   1) Select "TMS320F28335" of "2833X Delfino" from Variant under Main tab.

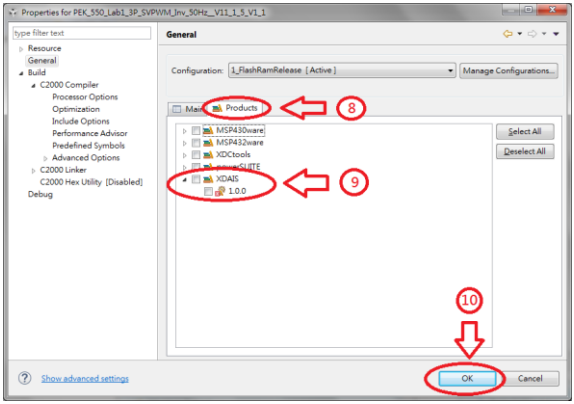
   2) Select "Texas Instruments XDS100v1 USB Debug Probe" from Connection under Main tab.

   3) Select "none" from Linker command file under Main tab.

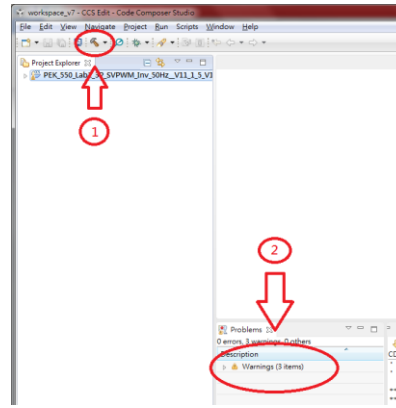
   4) Deselect "XDAIS" under Project tab. (Ignore this step if your CCS version doesn't provide this option.



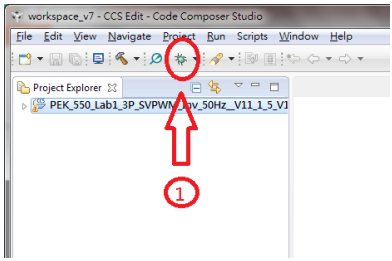




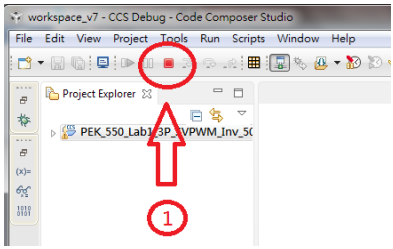
7. After the setting, click "Build" for compilation. If no errors occur after compiling, the program is eligible for burning. Simply ignore the warnings, which have no impact on burning process.



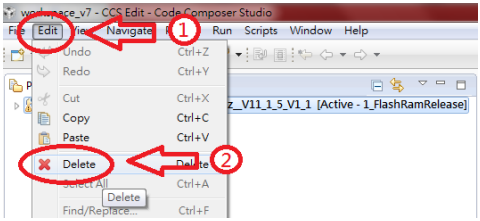
8. Connect PEK-006 to PC and PEK module respectively followed by clicking "Debug" to proceed to burning process.

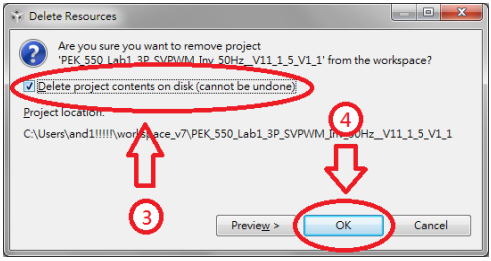


9. After the burning process, click "Terminate" and remove "PEK-006"to finish the entire procedure.



10. If it needs to delete file, select C Code file followed by selecting "Delete" under "Edit" tab and checking "Delete project contents on disk". Finally, click "OK" to complete the action.



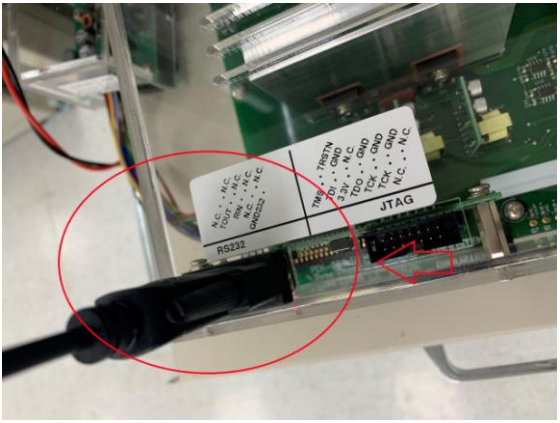


Appendix C – RS232 Connection

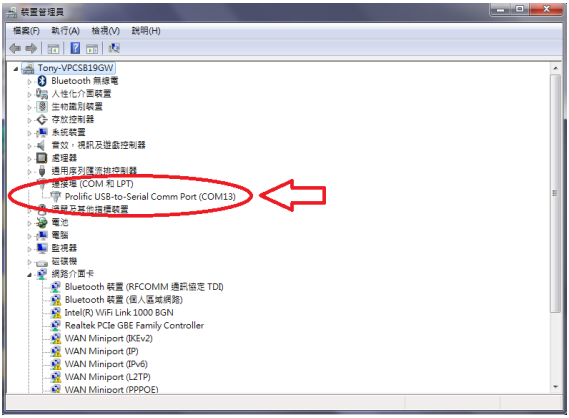
Operating steps

1. Connect PEK-005A to PEK module and make sure DSP is working normally.

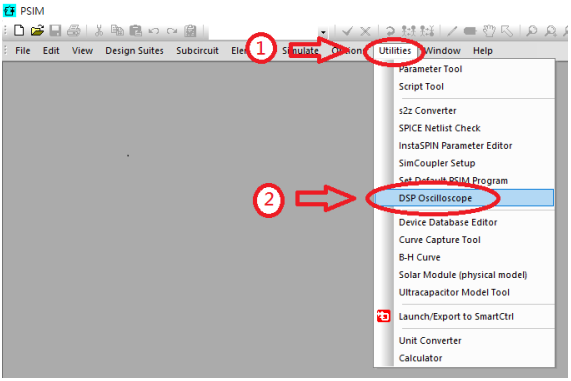
2. Connect one end of RS232 cable to PC, and the other end to the RS232 connector of PEK module.



3. Open Device Manger from PC and identify the COM port number being utilized by RS232 cable.



4. Open PSIM program and select “DSP Oscilloscope” under “Utilities” tab.

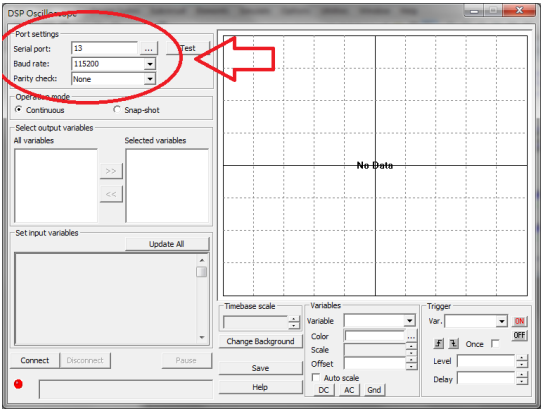


5. The Port settings are as follows.

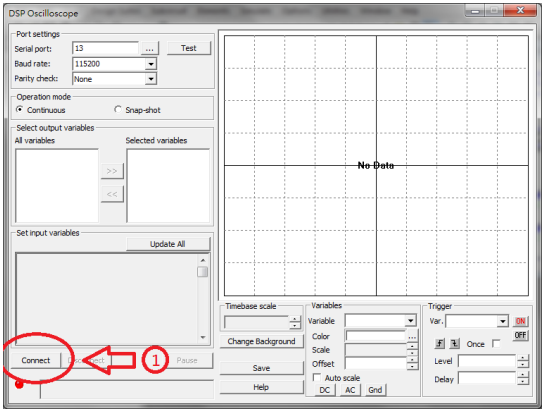
   1) Select the COM port being used by RS232.

   2) Set 115200 for Baud rate.

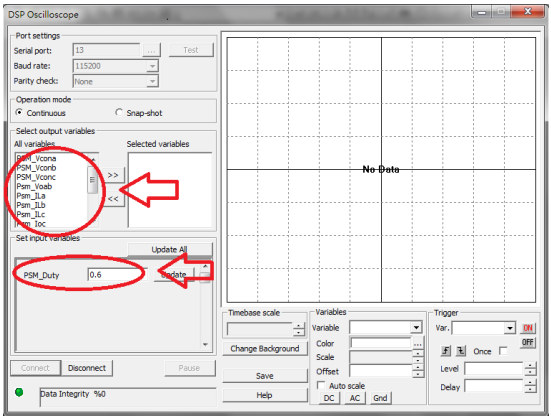
   3) Set None for Parity check.



6. After the settings, click "Connect" to proceed to RS232 connection.



7. Both the output and input variables schemed within PSIM circuit can be clearly observed when connection is properly established.



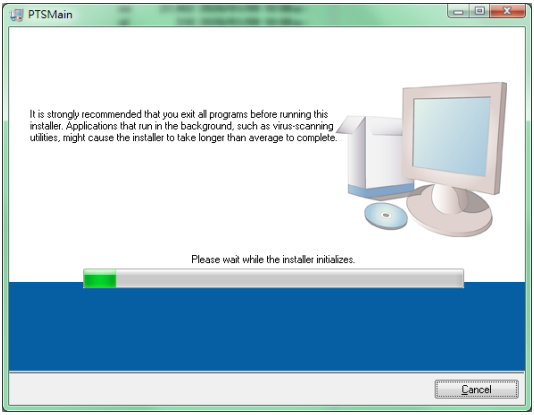
Appendix D – SAS Operation Procedure

We thoroughly introduce the PTS software covering SAS signal tracking, BAT simulation and real-time signal measurement subsystem. Through the system auto-detection function, each device can be well applied to the corresponding functions.

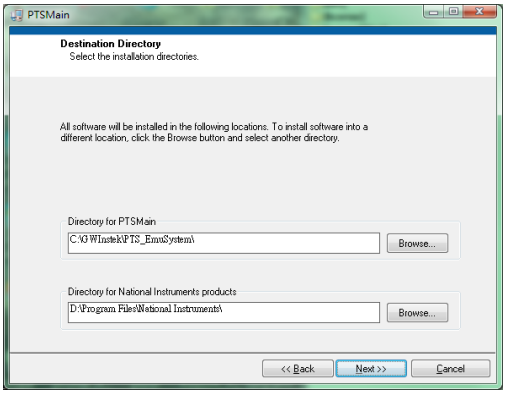
Installation and Startup

Operating steps

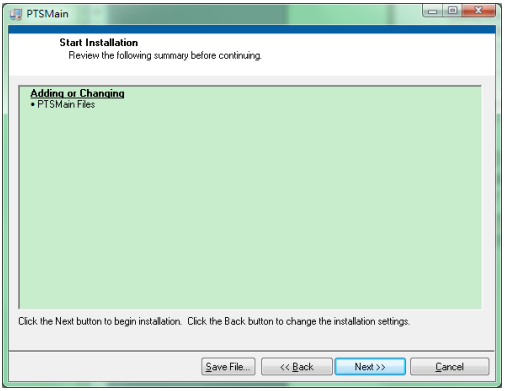
1. Install the complete PTS software: download the PTS5 installer and decompress it to the location c:\PTS installer followed by entering the Volume and executing the Setup.exe as follows.



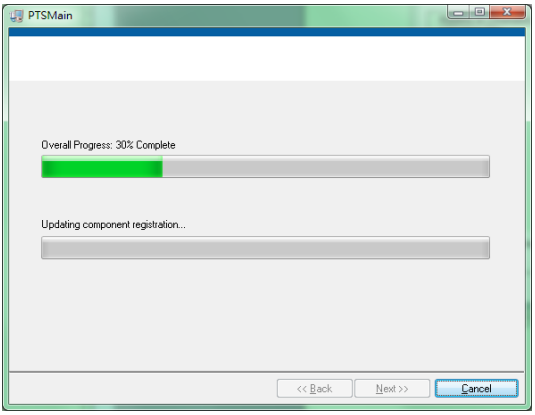
2. The system will search if the required component has been installed. If the required component is not installed yet or the installed one is with old version, the required component will be in the waiting list for installation. In contrast, if the installed one is with higher version than the required one, the installation process will be skipped.



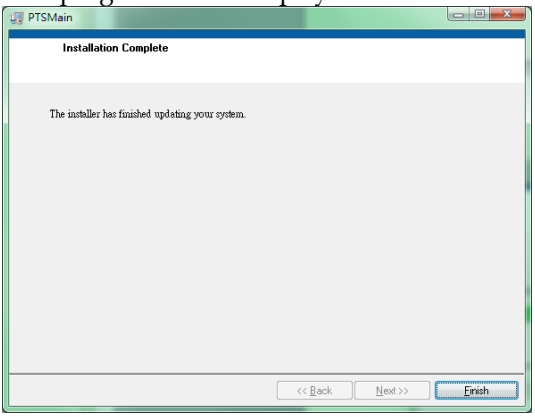
Use the default location and press the "Next" to finish installation. Then, the installed software and the software waiting to be installed including the required executing component will be listed.



3. Press "Next" to proceed to the following installation.

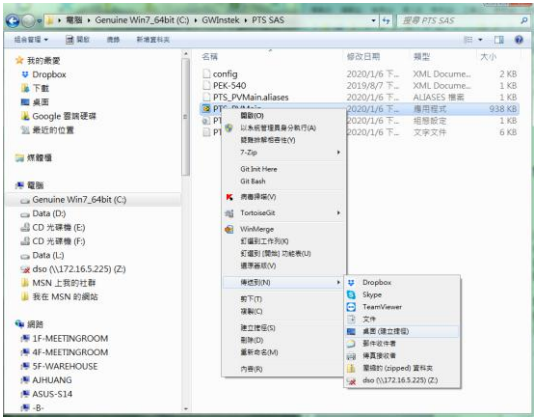


The overall installation progress along with each item progress will be displayed.



4. Download the PTS SAS package software and decompress it to the previous location for installation. A new directory will be added under the location c:\gwinstek\.

5. Switch to the directory and it is available to create a shortcut on the desktop for convenient execution. See the following screenshot shown.



Right click on the PTS_PVMain file followed by selecting “Sent to” -> “Desktop (create shortcut)” to create a shortcut, which allows you to promptly execute the software from the desktop directly with ease.

6. Locate the shortcut from desktop and execute it promptly when necessary later.

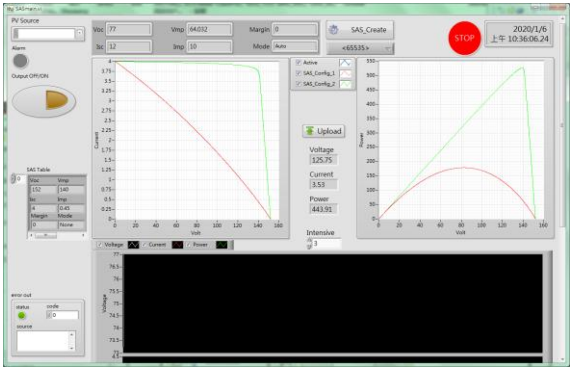
Uninstall

7. In the Control Panel, click the “Programs and Features” item followed by locating the PTSMain one for uninstall.

Interface Introduction

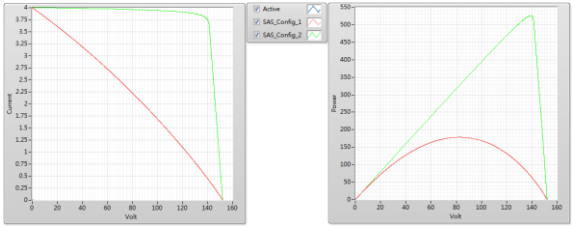
Program Running Interface

Diagram 1 System Running Interface



The PV trajectory curve of the configured system

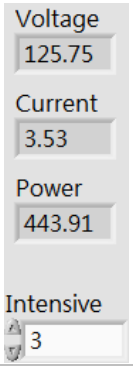
Diagram 2



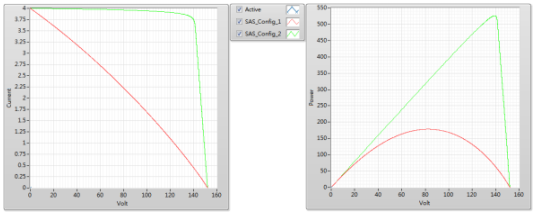
V1 display in left and PV display in right. Active indicates the one after startup. The real IV measurements, via Intensive setting, allow user to check the relevant trajectories.

Real-time readings monitor

Diagram 3



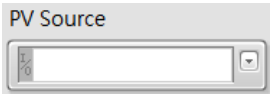
Both Voltage and Current are indicated in the left side of the IV curve chart from the diagram 2, whereas both Voltage and Power are indicated in the right side of the PV curve chart from the figure 2. Intensive indicates the remaining data points on screen, which tracks the real IVP fluctuating trajectory.



Operation

Device connection setup

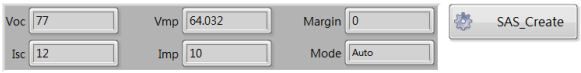
Diagram 4
Device selection



Establish system connection, via the drop-down menu, to designate the applicable device.

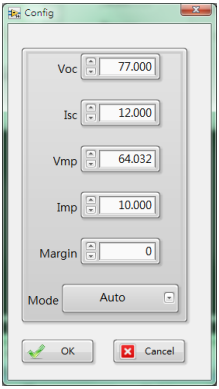
Establish PV reference curve

Diagram 5
Trajectory parameters of previous setup



8. SAS_Create: Establish a new curve as the following screenshot shown:

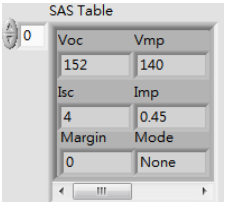
Diagram 6 SAS trajectory parameter setting



When a new curve is established, the relevant curve will be displayed in the VI and PV charts. And it is available to add parameters for the curve into the SAS table.

- Voc: Open circuit voltage
- Isc: Short circuit current
- Vmp: Max power point voltage
- Imp: Max power point current
- Margin: Output will not be updated within the ample area (%)
- Mode: Select Auto mode when utilizing
- OK: Confirm parameter setting and import into SAS Table
- Cancel: Discard the modification setting

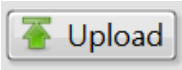
Diagram 7 Trajectory parameter table



- SAS Table: The curve ready to be written into device. Right click to open the operational functions: Import Table, Export Table
- Import Table: Load the previously established curve and parameter in the auto-saving file.
- Export Table: Export the current curve and parameter. Point the cursor to the SAS Table, through the delete button, to delete the current setting (trajectory curve).

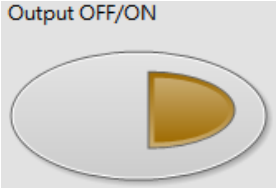
Upload / Load PV trajectory curve parameter

Diagram 8



Write the set trajectory curve parameter from the SAS Table into the device and wait for execution. In the meantime, PSW enters the SAS running mode.

Diagram 9



Start / Stop PSW output
In the SAS mode, PSW output reacts in accord with the selected curve. In the normal mode, PSW acts as a standard function.

Select Trajectory Parameter

Diagram 10

Refer to trajectory parameter selection

Stop and End

Diagram 11

Once the upload action is executed, the device enters the SAS mode and all the Output ON/OFF control determine if PSW proceeds to tracking operation.

If PSW requires to returning back to the normal operation mode, it must select stop software and restart it.

Appendix Description

A: PSW Tracking Mode

After SAS software startup, PSW will, by uploading trajectory curve software, initiate tracking mode. User then is able to switch freely among the established trajectory software. In order to exit from the tracking mode, press the "STOP" to make the device return back to the default operation mode.

B: Normal Mode

System is under the normal operation mode after startup. PSW enters the tracking mode after successfully uploading the PV trajectory curve.

C: IVP Real-Time Record Curve

In the tacking mode, apart from IV and PV trajectories, the both trajectory record charts are also provided, individually.

Diagtam 12

9.